Schneider TV·VIDEO

Stereo-Fernseh-Empfänger
DIGITAL
DTV 2

CTM 70

Serviceanweisung
Service manual

Achtung!

Bei Reparaturen unbedingt Trenntrafo benutzen und gültige Sicherheitsvorschriften beachten. Die Netzsicherung befindet sich auf der Netzschalterplatine.

Röntgenverordnung

Die in der Röntgenverordnung festgelegte Ortsdosisleistung ist bei diesem Gerät durch die Bildröhrentype und die maximal zulässige Hochspannung gewährleistet. Die Hochspannung darf maximal 27,5 kV betragen. Die Hochspannung liegt im zulässigen Bereich, wenn die Betriebsspannung der Horizontal-Ablenkstufe bei minimalem Strahlstrom 148 V beträgt. Bei Reparaturen ist die Spannung zu überprüfen und gegebenenfalls mit R 226 auf Sollwert einzustellen.

Wichtig:
Bevor das Gerät auf »Service-Mode« geschaltet wird, müssen vorhandene Gerätefehler beseitigt sein.
Bei Austausch der kompletten Digitalplatine ist eine neue Grundeinstellung notwendig.
Achtung: Die üblichen Vorschriften zum Schutz statischer Aufladungen müssen dabei unbedingt eingehalten werden.
Werkseitig werden die Daten für ein Gerät mit 56-cm-Bildschirm eingelesen.

Vorbereitung:
Das Gerät ist vor Umschaltung in den Service-Mode auf einen Kanal mit Kombi-Testbild einzustellen.
Alle Abgleichvorgänge im Service-Mode (außer Punkt 1, 2 und 11) sind bei geschlossenem Gerät mit der Fernbedienung möglich.

Service-Mode aufrufen:

1. Servicetaste gedrückt halten (siehe Fig. 1).
2. Taste »C« kurz antippen.
3. Servicetaste lösen.
4. Beliebige Programmtaste drücken.

In der Bildschirmmitte erscheint dann die Einblendung »SERVICE MODE«.
Jetzt können die verschiedenen Abgleichpunkte mit der Fernbedienung aufgerufen, verändert und jeder einzelne Abgleichvorgang gespeichert werden.

Tasten BASS	−+	= Abgleichpunkt aufrufen
Tasten VOLUME	−+	= Einstellung verändern
Taste Ideal		= Einstellung speichern

Zur nachfolgenden Tabelle sind noch folgende Hinweise zu beachten:
a) Für die Service-Einstellung werden nur die in der nachfolgenden Tabelle aufgeführten Abgleichpunkte benötigt.
b) Folgt hinter einem großen ein kleiner Buchstabe, bedeutet dies die Feineinstellung, während ein Großbuchstabe an 2. Stelle die Grobeinstellung signalisiert.

Bei Bildröhren- und Bildrohrplatinenwechsel muß unbedingt die Beschaltung des Ablenksteckers (Schaltbild Ablenkteil) und der Wert des Heizwiderstandes R 1635 (siehe Tabelle für Bildröhre und Bildrohrplatine) verglichen werden.

Warning!

Always use an isolating transformer for repair works and adhere to existing safety regulations. The power supply fuse is located on the power switch board.

X-ray regulations

The picture tube type and the maximum permissible high-voltage ensure that the X-ray intensity within the set remains far below the permissible value.
The high-voltage must not exceed 27.5 kV. The high-voltage is within the permissible limits when the operating voltage of the horizontal deflection stage equals 148 V at minimum beam current. Following servicing, check and adjust this voltage to the nominal value with R 226.

Important:
Before the set is switched to "service mode" any faults in it must be cleared.
New basic settings will be necessary if the complete digital PC board is exchanged.
Important note: Compliance with the generally valid rules for protection against static charges is essential.
The data entered in the factory applies to a set with a 56 cm screen.

Preparation:
Before being switched to the service mode the unit must be set to a channel with a combined test pattern.
All adjustments in Service-Mode (without point 1, 2 and 11) are possible with the remote control and closed unit.

Calling Service-Mode:

1. Keep pressing service button (see Fig. 1).
2. Tip button "C".
3. Loose service button.
4. Press anyone program button.

"SERVICE-MODE" will then appear in the centre of the screen.
The various adjustment points can then be called and altered with the remote control unit, and each adjustment procedure stored.

BASS buttons	−+	= Call adjustment point
VOLUME buttons	−+	= Adjust setting
Ideal button		= Store setting

Notes on the table below:
a) Only the adjustment points listed in the table below are required for the service setting.
b) An upper-case letter followed by a lower-case letter indicates a fine setting, whilst the opposite sequence indicates a coarse setting.

When replacing the picture tube or the picture tube PC board, it is essential to compare the wiring of the deflection plug (see circuit diagram of deflection unit) with the heating resistance R 1635 (shown table of picture tube and picture tube PC board).

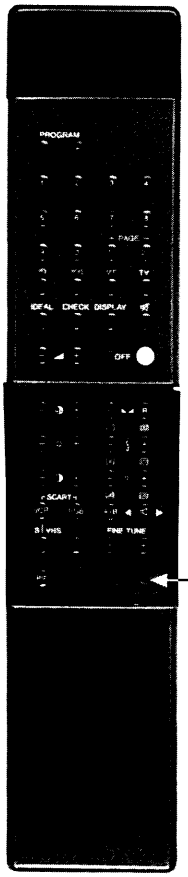
	Abgleichvorgang	Bildschirm-Anzeige	Bemerkung
1.	Betriebsspannung		Mit R 226 auf dem Ablenkchassis wird U 1 148 V ± 0,5 V eingestellt.
2.	Focus		Mit dem Focus-Regler auf der Bildrohr-Platine optimale Bildschärfe einstellen.
	Die folgenden Einstellungen sind nur im Service-Mode möglich. **Jeder einzelne Abgleichvorgang muß mit Taste »Ideal« (Geber) gespeichert werden.**		
3.	Bildlage, horizontal	SP	Bild so zentrieren, daß die Randüberschneidungen möglichst gering sind (Service-Balken zentrieren).
4.	Bildlage zentrieren	BP	Testbild symmetrisch einstellen.
5.	Bildlage vertikal	AO	Gittermuster so einstellen, bis Meßzeile am oberen Bildrand verschwindet.
6.	Amplitude vertikal grob Amplitude vertikal fein	HO Ho	Wechselseitig optimal einstellen (evtl. Ao nochmal nachgleichen).
6a.	Linearität	SO So SI Si	Wenn erforderlich, Hilfstabelle für Bildröhren verwenden.
7.	Amplitude horizontal	YO	Nur bis ca. 2 cm vom Bildschirmrand einstellen (evtl. auf Minimum).
8.	o/w Kissenentzerrung (zu groß) o/w Kissenentzerrung (zu klein) ZO PO	ZO Zo PO Po	Mit ZO auf ca. 2 stellen (evtl. Bild stark verzerrt). Mit PO Bild wieder einstellen. Ist Kissen zu groß, ZO-Anzeigewert schrittweise größer stellen und mit PO wieder einstellen. Bei zu kleinem Kissen ZO kleiner stellen und mit PO nachjustieren. Mit Zo leichte Entzerrungen justieren.
8a.	Kissen	ZI Zi PI Pi	Wenn erforderlich, Hilfstabelle für Bildröhren verwenden.
9.	Amplitude horizontal	YO	Abschließend nochmal die Bildbreite einstellen.
10.	FO. Farbe	SA	FHT einstellen, bis Farb-Jalousie von Senkrecht- auf Waagrecht-Durchlauf umspringt.
11.	G2 Helligkeit + Kontrast	G 2	Mit G2-Regler auf der Bildrohr-Platine Helligkeit und Kontrast optimal zwischen MIN und MAX einstellen.
12.	R G B Schwarzabgleich	CR CG CB	Nach korrekter G2-Einstellung wird automatisch die empfindlichste Kathode ermittelt. Sie wird als Referenz für die 2 anderen Farbsysteme benutzt und kann nicht verändert werden. Das heißt, daß nur die beiden fehlenden Farben geregelt werden können. Diese müssen durch Versuch ermittelt werden.
13.	R G B Weißabgleich	DR DG DB	Nur die dominierenden Farben nachregeln. Eine Farbe sollte immer in der Grundstellung bleiben.
	Nach Beendigung der Service-Einstellungen wird durch Drücken der Taste »TV« wieder auf TV-Betrieb geschaltet.		
	Bei Ausführung Multinorm ist mit NTSC-Testbild Abgleichvorgang 3 bis 9 (Geometrie) separat durchzuführen.		
	Bildlage bei RGB-Eingang: Abgleichvorgang 3 und 4 kann separat eingestellt werden (Testbild über RGB eingeben. Service-Mode aufrufen).		
	Bildlage bei Video-Eingang: Abgleichvorgang 3 und 4 kann separat eingestellt werden (Testbild über Video eingeben, Service-Mode aufrufen).		
	Bildlage horizontal bei Videotext justieren: Service-Taster (auf Digitalplatine) und Taste »VT« (Fernbedienung) bei Fernsehempfang gleichzeitig drücken. Bildlage horizontal mit Tasten »Lautstärke + und –« justieren. Einstellung mit Taste »Ideal« (Fernbedienungsgeber) speichern.		

Abgleich für Geometrie nach Tabelle:

Bei Einstelländerung eines Abgleichpunktes wird in der Service-Mode-Zeile der Zahlenwert eingeblendet.
Die Einstellwerte der verschiedenen Röhrentypen können aus der Tabelle entnommen werden. Die angegebenen Werte sind Annäherungswerte und sind von Toleranzen abhängig.

Geometry adjustments according to table:

If the setting of an adjustment point is altered, the numeric value appears in the service mode line.
The settings for the various types of tube can be taken for the table. The specified values are approximate and are subject to tolerances.



Servicetaste
Service button

Fig. 1

Bildröhre Picture tube	Standard	Anzeige im Service Mode – Indication Service Mode					
		SO	So	SI	Si	ZI	PI
A 51 EAF 00X01 R 35 = 2,2 Ω	Pal/Secam	9	127	0	191	0	0
	NTSC	0	112	1	1	0	0
A 56-701 X R 35 = 2,2 Ω	Pal/Secam	1	64	0	200	0	2
	NTSC	0	110	0	6	0	25
A 59 EAF 00X01 R 35 = 2,2 Ω	Pal/Secam	1	64	0	200	0	0
	NTSC	22	72	0	240	0	0
A 59 EAK 00X01 R 35 = 5,6 Ω	Pal/Secam	1	64	0	200	0	13
	NTSC	0	112	1	1	1	110
A 63 NCQ 00X08 R 35 = 2,2 Ω	Pal/Secam	1	64	0	200	0	0
	NTSC	0	2	1	0	0	10
A 66 EAF 00X01 R 35 = 2,2 Ω	Pal/Secam	1	20	0	20	0	2
	NTSC	2	76	0	0	0	2
A 66 EAS 00X01 R 35 = 2,2 Ω	Pal/Secam	1	64	0	200	0	6
	NTSC	0	112	1	0	0	26
A 66 EAK 00X01 R 35 = 5,6 Ω	Pal/Secam	1	64	0	200	0	7
	NTSC	0	90	0	0	0	30
A 66 EAK 50X01 R 35 = 5,6 Ω	Pal/Secam	1	50	0	200	0	4
	NTSC	0	110	1	1	0	26
A 66 ECF 00X01 300 mA (Code Röhrenhals 8...) R 35 = 5,6 Ω	Pal/Secam	1	0	0	20	0	4
	NTSC	1	110	0	8	0	12
A 66 ECF 09X01 R 35 = 2,2 Ω	Pal/Secam	1	64	0	200	0	0
	NTSC	0	110	0	8	0	33
M 78 JUA 98X01 R 35 = 2,7 Ω	Pal/Secam	1	26	0	21	0	5
	NTSC	2	102	0	4	0	8

Hinweis zum Schaltbild:

Die Bauteile werden grundsätzlich mit Vornummern gekennzeichnet.

Vornummer 1: Netzteil auf Netzplatine
Vornummer 2: Netzteil auf Ablenkchassis
Vornummer 3: Horizontal-Endstufe auf Ablenkchassis
Vornummer 4: O/W-Endstufe auf Ablenkchassis
Vornummer 5: Vertikal-Endstufe auf Ablenkchassis
Vornummer 6: Videotext-µP auf Digichassis
Vornummer 7: Ablenk-µP auf Digichassis
Vornummer 8: Scart auf Digichassis
Vornummer 9: Audio-Endstufe auf Digichassis
Vornummer 10: Audio-µP auf Digichassis
Vornummer 11: Videoaufbereitung auf Digichassis
Vornummer 12: Tuner, PLL und ZF-Anschluß auf Digichassis
Vornummer 13: Zentrale Steuereinheit auf Digichassis
Vornummer 14: Multi-Scart-Platine
Vornummer 15: Bedienteil, IR-Empfänger
Vornummer 16: Bildrohrplatine
Vornummer 17: ZF-Modul Standard B/G
Vornummer MA 17: Audio-Modul auf ZF-Multinorm
Vornummer MVL 17: Video-Logik-Modul auf ZF-Multinorm
Vornummer 18: Single-Scart-Platine

zum Beispiel: IC 1 im Netzteil ≙ IC 201
IC 1 in Vertikalstufe ≙ IC 501
Widerstand CR 12 in O/W-Stufe ≙ Chip-Widerstand 412

Hint to circuit diagram:

The electrical parts have to be marked with a key-number.

Key number 1: power supply on power switch P.C.B.
Key number 2: power supply on deflection P.C.B.
Key number 3: horizontal out on deflection P.C.B.
Key number 4: E/W out on deflection P.C.B.
Key number 5: vertical out on deflection P.C.B.
Key number 6: teletext µP on digi P.C.B.
Key number 7: deflection µP on digi P.C.B.
Key number 8: scart on digi P.C.B.
Key number 9: audio out on digi P.C.B.
Key number 10: audio µP on digi P.C.B.
Key number 11: video on digi P.C.B.
Key number 12: tuner, PLL and IF-connector on digi P.C.B.
Key number 13: central circuit unit on digi P.C.B.
Key number 14: multi scart P.C.B.
Key number 15: control P.C.B. with IR receiver
Key number 16: picture tube P.C.B.
Key number 17: IF-modul standard B/G
Key number MA 17: audio modul on IF multi standard
Key number MVL 17: video logic modul on IF multi standard
Key number 18: single scart P.C.B.

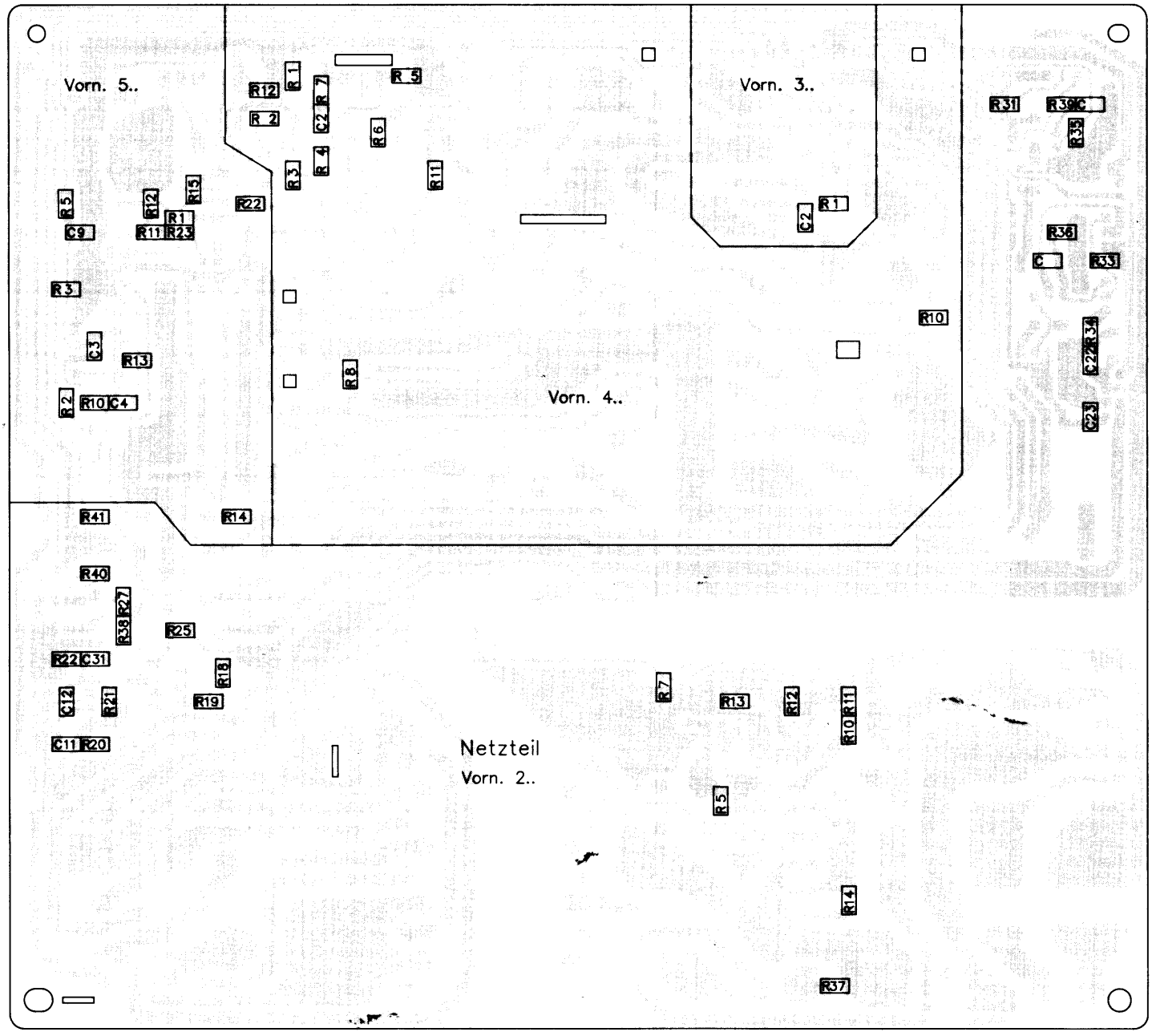
for example: IC 1 on power supply deflection P.C.B. ≙ IC 201
IC 1 on vertical out ≙ IC 501
Resistor CR 12 on E/W-out ≙ Chip resistor 412

	Adjustment procedure	Screen indication	Remarks
1.	Operating voltage		Set U 1 148 V ±0.5 V with R 226 on deflection chassis.
2.	Focus		Set optimum picture definition with focus control on picture tube PC board.
	The following settings can only be made in service mode. **Each adjustment has to be stored with button "Ideal" (remote control).**		
3.	 Horizontal centring	SP	Centre picture to obtain minimum edge overlapping (centre service bar).
4.	 Picture centring	BP	Make test pattern symmetrical.
5.	 Vertical centring	AO	Adjust grid pattern until measurement line at top picture margin disappears.
6.	 Vertical amplitude, coarse Vertical amplitude, fine	HO Ho	Adjust alternately to optimum setting (readjust AO if necessary).
6a.	 Linearity	SO So SI Si	Use table of picture tube, if necessary.
7.	 Horizontal amplitude	YO	Adjust only to approx. 2 cm from picture margin (to minimum, if necessary).
8.	 E/W Pin cushion (too large)  E/W Pin cushion (too small)  ZO  PO	ZO Zo PO Po	Set ZO to 2 (picture is distort). Adjust picture with PO. If pin cushion is too large, set ZO one point higher and adjust PO once more. If pin cushion is too small, set ZO one point lower and adjust PO once more. Zo is for easy adjustment.
8a.	 Pin cushion	ZI Zi PI Pi	Use table of picture tube, if necessary.
9.	 Horizontal amplitude	YO	Adjust picture width once more.
10.	 Colour	SA	Adjust FHT until colour test pattern changes from vertical to horizontal sweep.
11.	 Brightness + contrast	G 2	Set optimum brightness and contrast between MIN and MAX with G2 control on picture tube PC board.
12.	 Black adjustment	CR CG CB	If the G2 setting is correct, the most sensitive cathode is determined automatically. It is used as a reference for the other two colour systems and cannot be altered. This means that only the other two colours can be adjusted. They must be determined by trial and error.
13.	 White adjustment	DR DG DB	Readjust only dominant colours. One colour should always be left at its basic setting.
	When all service settings have been made, press "TV" button to return to TV mode.		
	In the "Multinorm" version adjustment procedures 3 to 9 (geometry) must be performed separately with the NTSC test pattern.		
	Framing with RGB input: adjustment procedures 3 and 4 can be performed separately (enter test pattern via RGB, activate service mode).		
	Framing with video input: adjustment procedures 3 and 4 can be performed separately (enter test pattern via video, activate service mode).		
	Adjust horizontal centring with teletext: Press service pushbutton (on digi board) and "VT" pushbutton (remote control) simultaneously with television reception. Adjust horizontal centring with "volume + and –" buttons. Store setting with "Ideal" button (remote control unit).		

Ablenkteil
Deflection unit P.C.B.

Vornummer 2, 3, 4, 5
Key number 2, 3, 4, 5

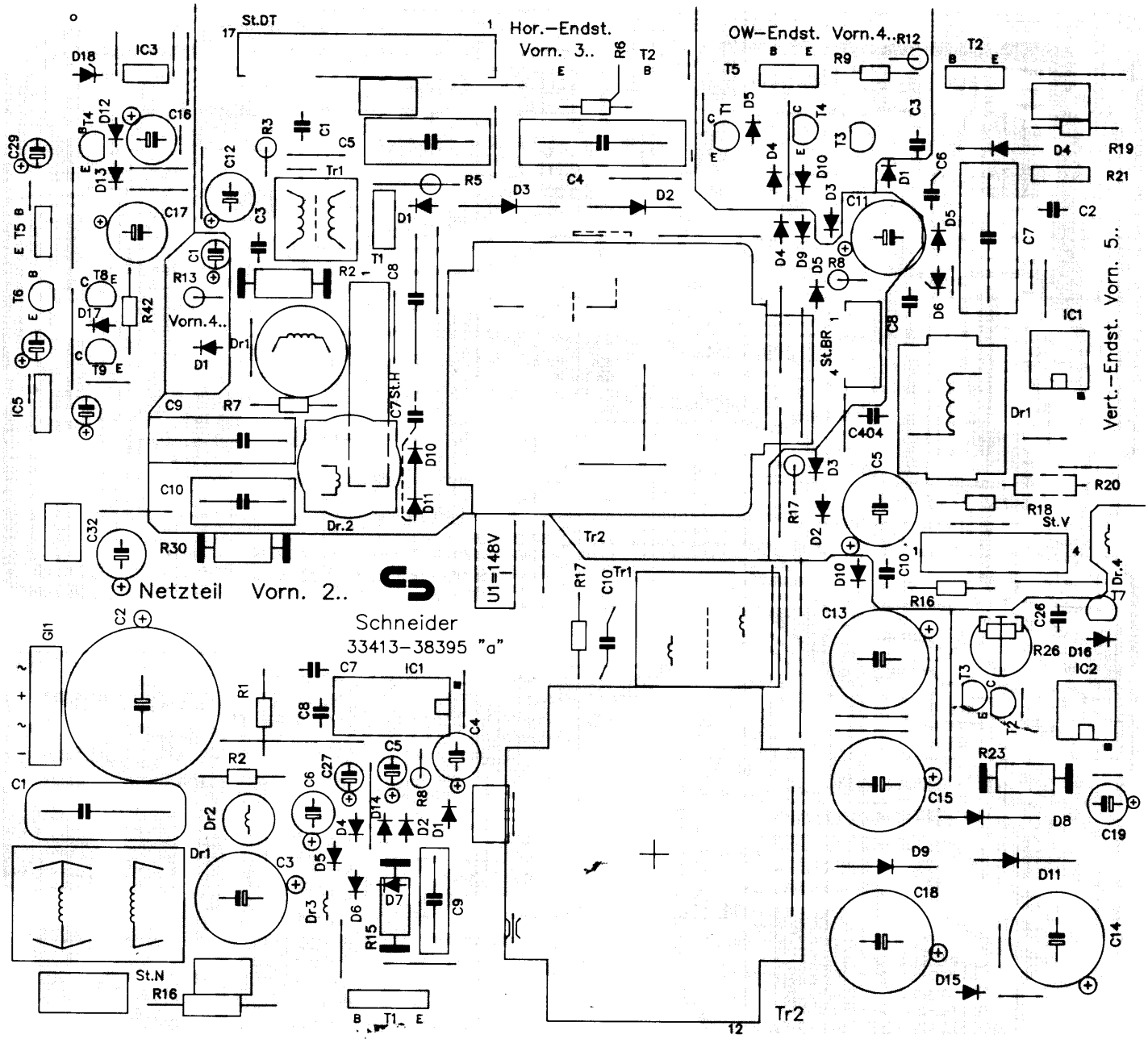
Chipseite
Bottom view



Ablenkteil
Deflection unit P.C.B.

Vornummer 2, 3, 4, 5
Key number 2, 3, 4, 5

Bestückungsseite
Top view



Schaltbild Ablenkteil
Circuit diagram deflection unit

⚠ Bei Servicearbeiten C 202 entladen!
For service discharge C 202!

Die Positionsnummern auf der Leiterplatte und dem Schaltbild sind mit der entsprechenden Vornummer zu ergänzen.

The position numbers on the P.C.B. and on the circuit diagram have to be completed with the corresponding key numbers.

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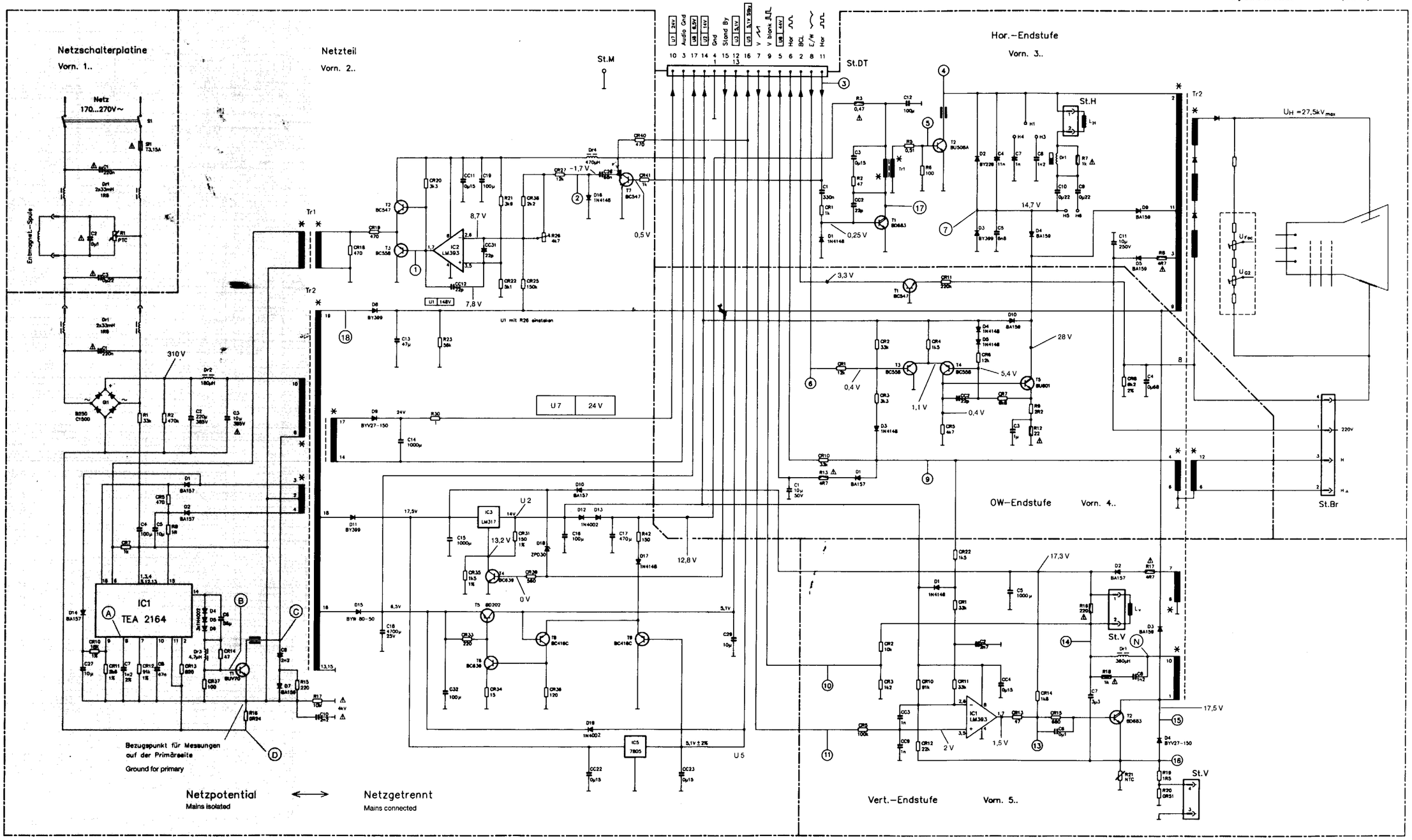
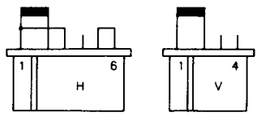
⚠ = Please use original spare parts only

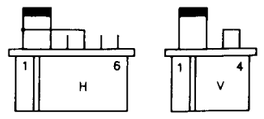


IC 201 TEA 2164		
Pin	ON	Stby.
9	2,2 V	2,8 V
10	2,5 V	4,5 V
14	0,5 V	1,2 V
15	10,7 V	8,2 V
16	11,3 V	12 V

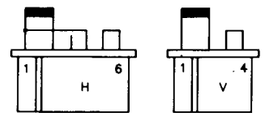
Beschaltung der Ablenkstecker
Wiring of deflection connectors



Videocolor	A56–701X
Videocolor	A67–701X
Videocolor	A66EAS00X01
SEL	A66EAF00X01
UNITRA	A56–701X
SEL	A56–701X



Valvo	A59EAK00X01
Valvo	A66EAK50X01
SEL	A66ECF00X01



Valvo	M78JUA98X01

Oszillogramme auf Rückseite Beiblatt!
Wave forms on back side of supplement!

Schaltbild ZF-Platine Multinorm
Circuit diagram IF multi-standard

Die Positionsnummern auf der Leiterplatte und dem Schaltbild sind mit der entsprechenden Vornummer zu ergänzen.

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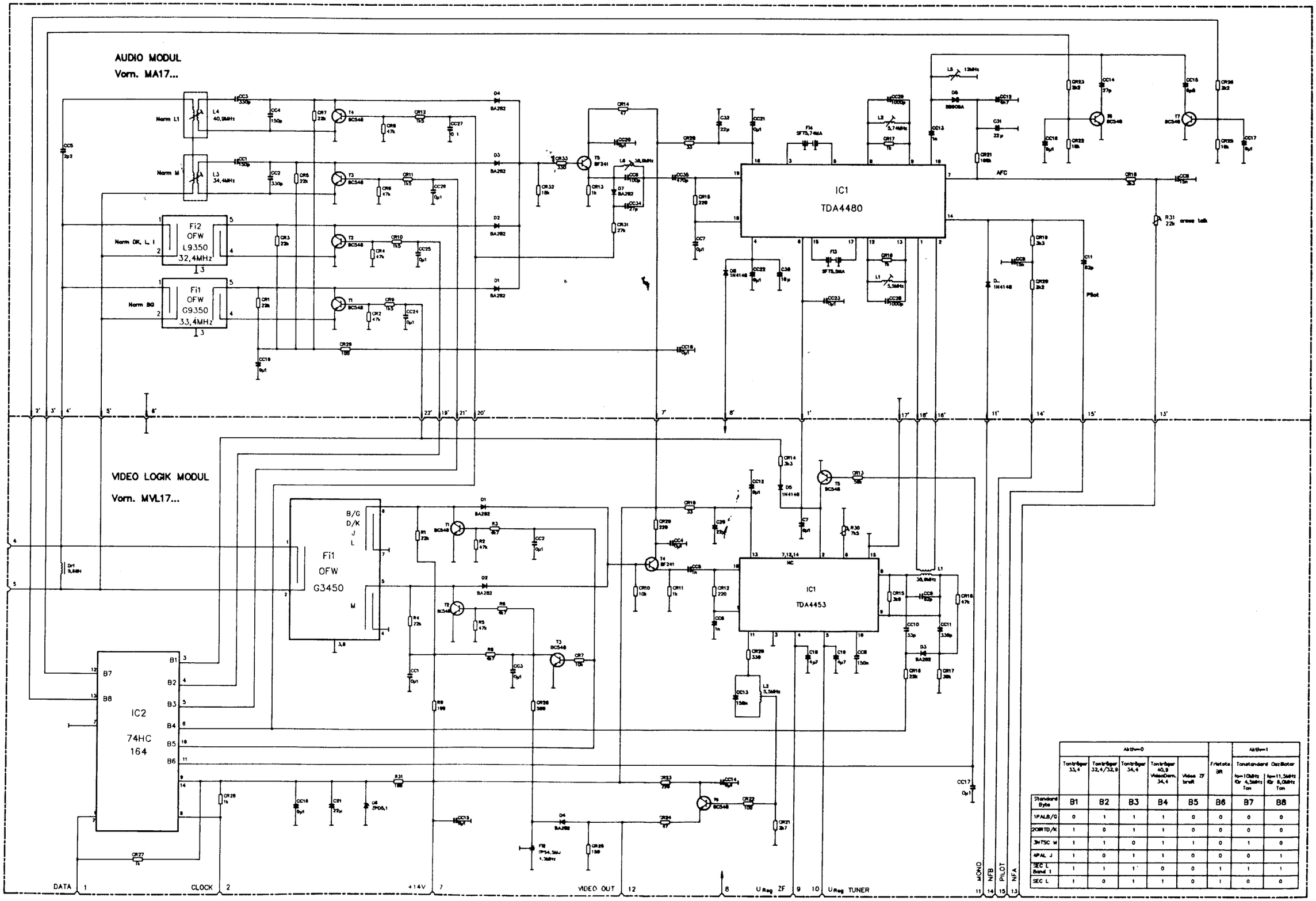
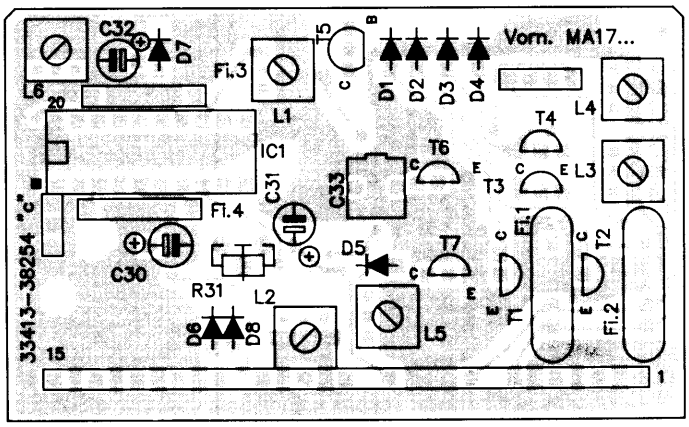


	Akth=0					Frietote BR	Akth=1	
	Tonträger 33,4	Tonträger 32,4/32,9	Tonträger 34,4	Tonträger 40,9 VideoDem. 34,4	Video ZF brutt		Tonstandard Oszillator fq=10,8MHz Kbr 4,5MHz Ton	fq=11,36MHz Kbr 6,0MHz Ton
Standard Byte	B1	B2	B3	B4	B5	B6	B7	B8
1PALB/G	0	1	1	1	0	0	0	0
2SECAM D/K	1	0	1	1	0	0	0	0
3NTSC M	1	1	0	1	1	0	1	0
4PAL J	1	0	1	1	0	0	0	1
SEC L Band 1	1	1	1	0	0	1	1	1
SEC L	1	0	1	1	0	1	0	0

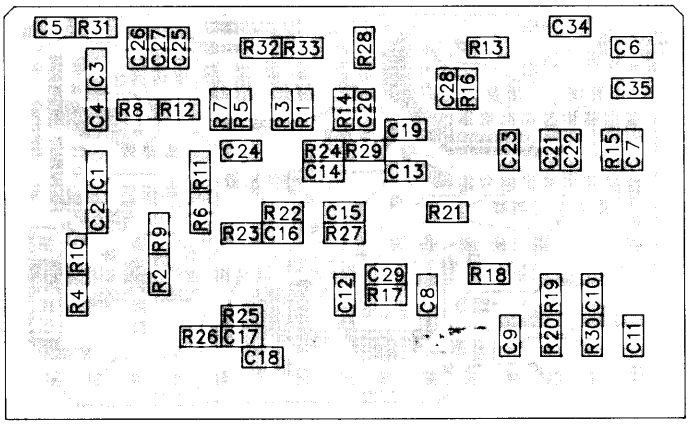
ZF-Platine Multinorm
IF P.C.B. multi-standard

Vornummer MA 17 . . .

Bestückungsseite
Top view

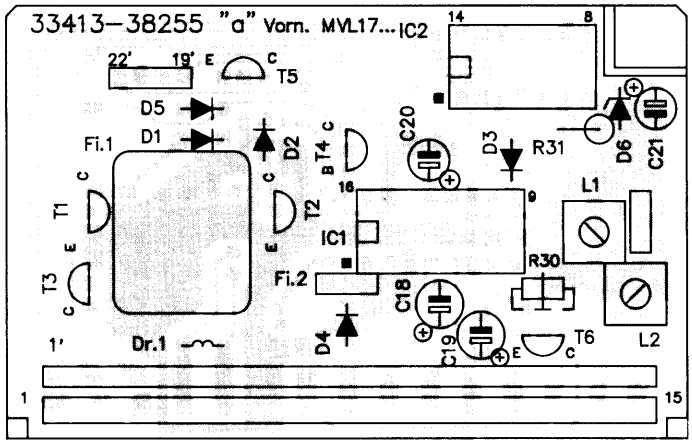


Leiterbahnseite
Bottom view

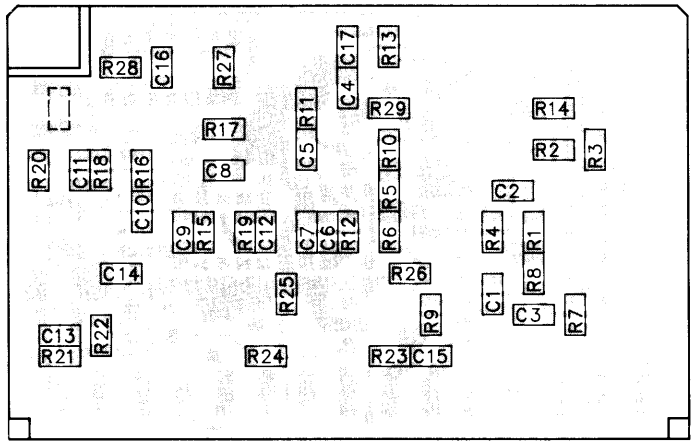


Vornummer MLV 17 . . .

Bestückungsseite
Top view



Leiterbahnseite
Bottom view



Schaltbild ZF-Platine Standard B/G
Circuit diagram IF Standard B/G

Die Positionsnummern auf der Leiterplatte und dem Schaltbild sind mit der entsprechenden Vornummer zu ergänzen.

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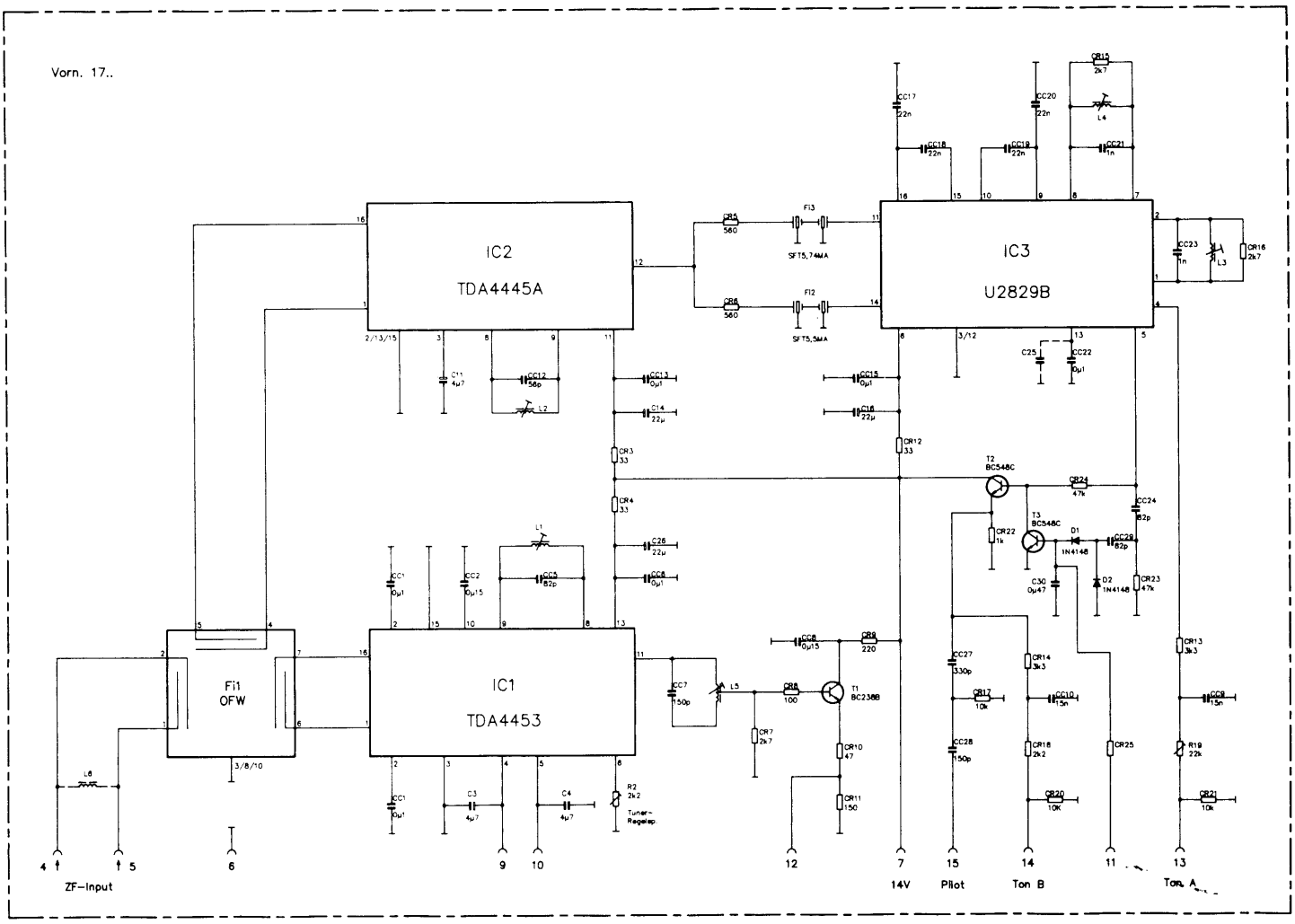
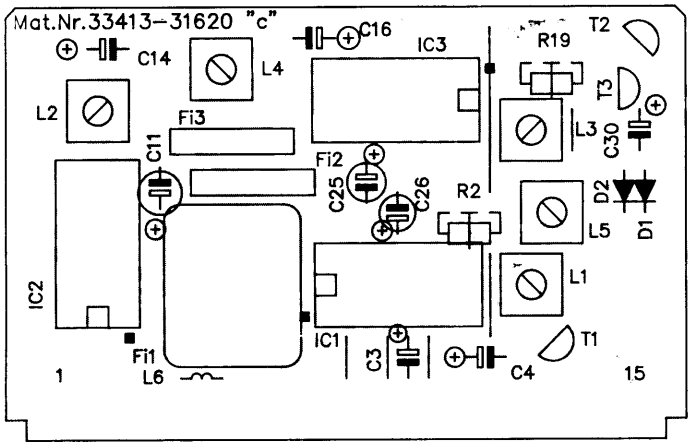


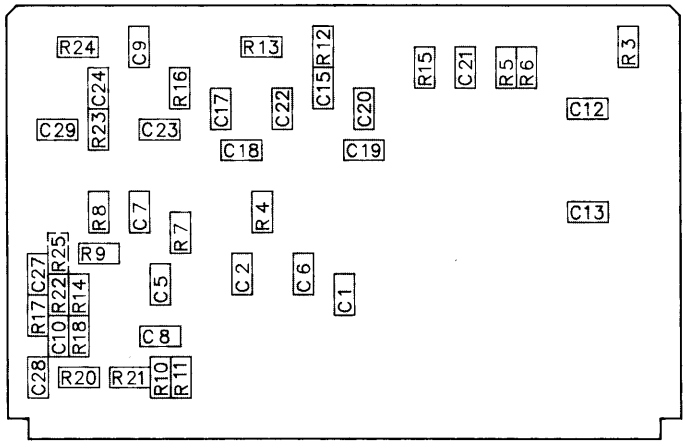
ZF-Platine B/G
IF P.C.B. B/G

Vornummer 17 . . .

Bestückungsseite
Top view



Leiterbahnseite
Bottom view



Schaltbild Bildrohrplatine
Circuit diagram picture tube board

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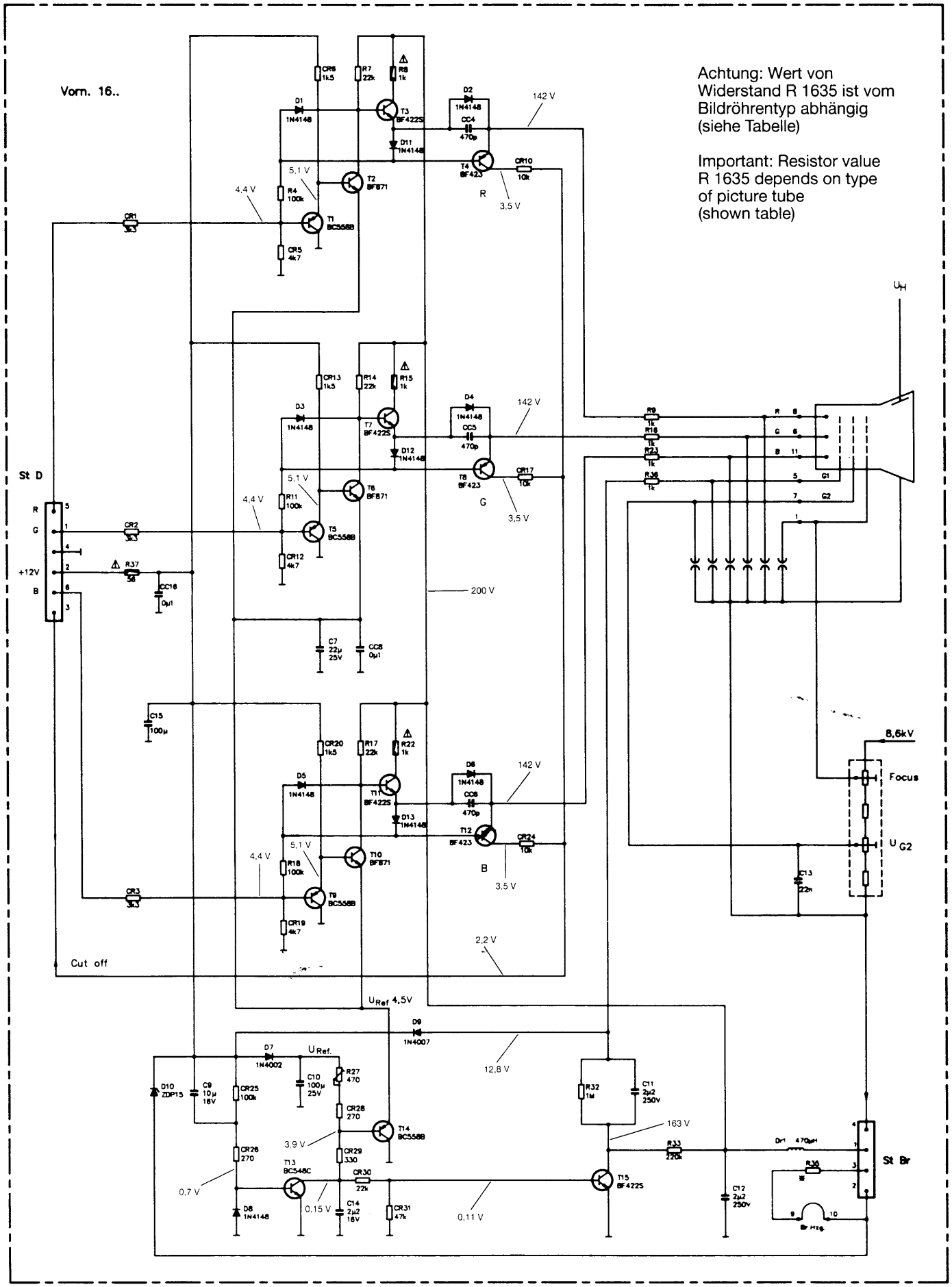
⚠ = Sicherheitsbauteile sind unbedingt durch Originalteile zu ersetzen

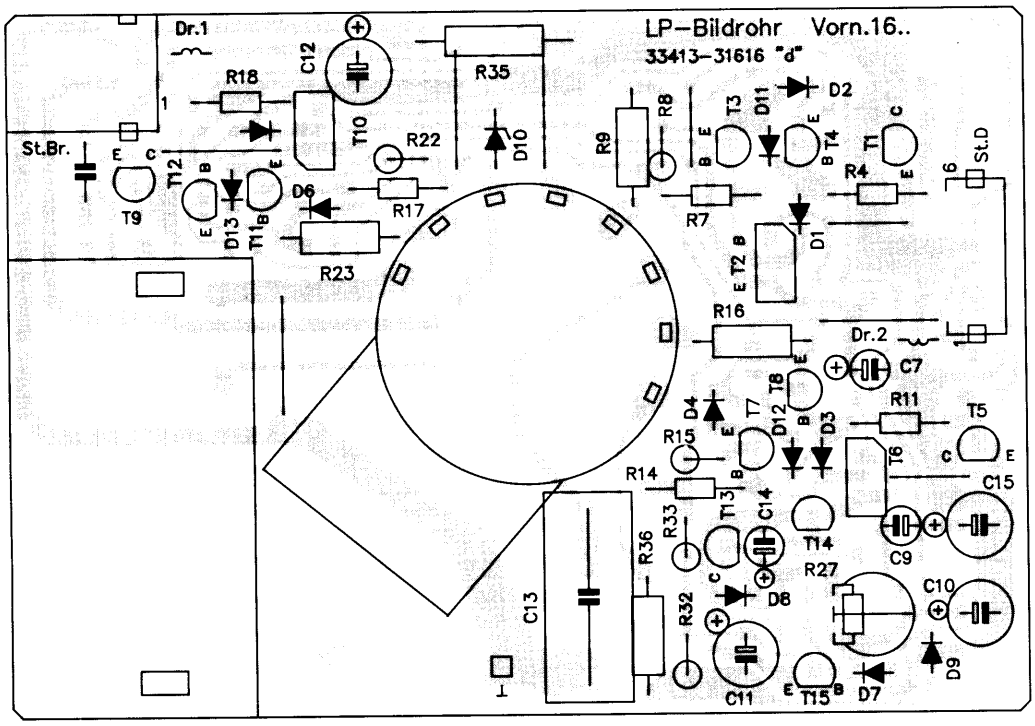
⚠ = Please use original spare parts only



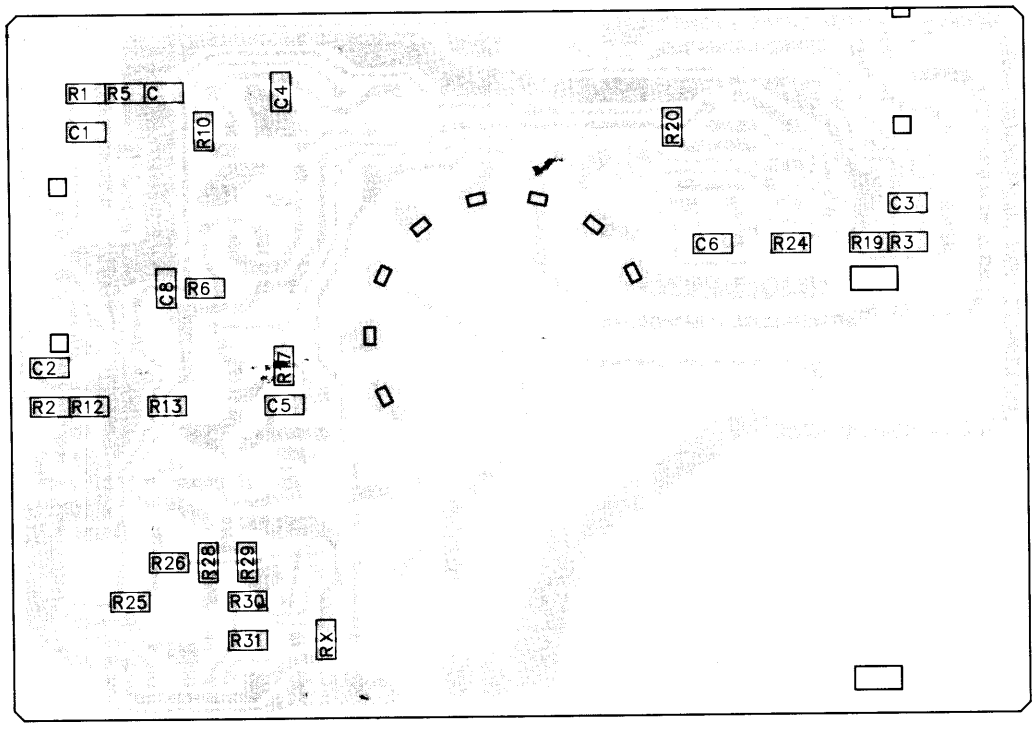
Bildrohrplatine
Picture tube P.C.B.

Vornummer 16 . . .
Key number 16 . . .

Bestückungsseite
Top view



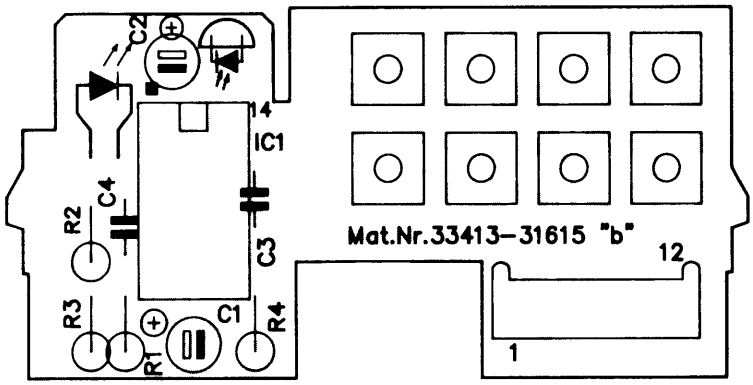
Leiterbahnseite
Bottom view



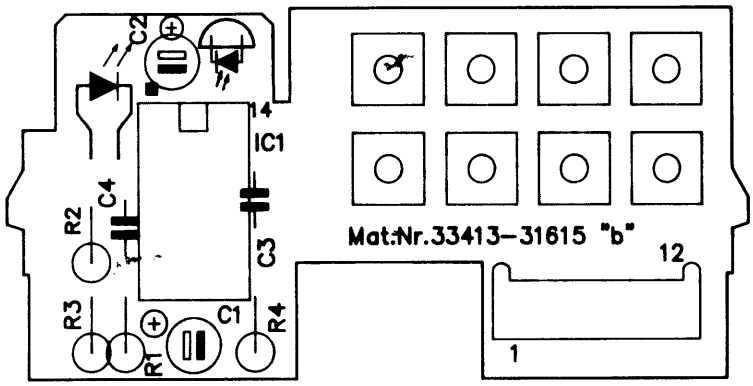
Bedienteilplatine
Control P.C.B.

Vornummer 15 . . .
Key number 15 . . .

Bestückungsseite
Top view



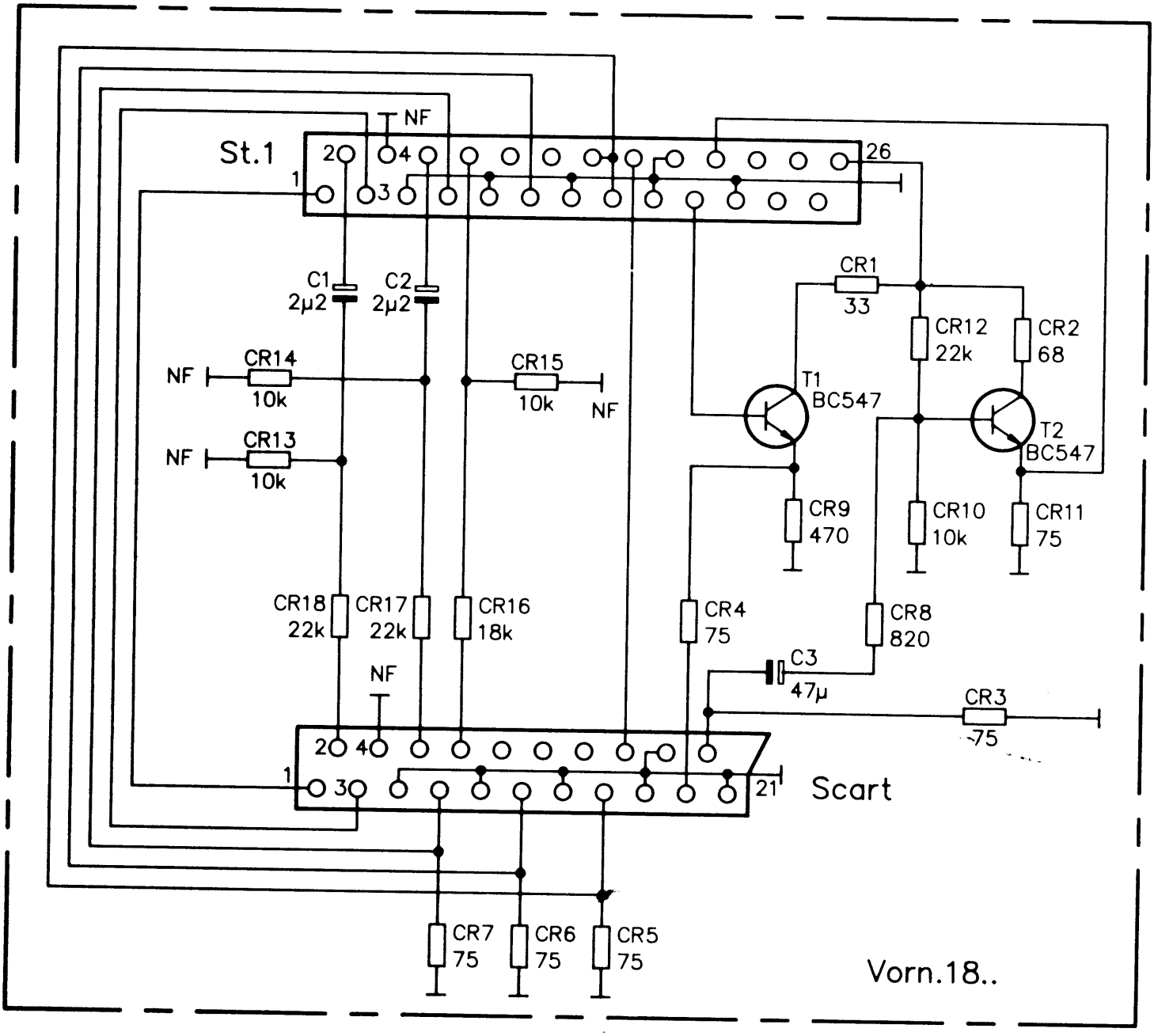
Bestückungsseite und Leiterbahndarstellung Lötseite
Top view with layout soldering side



Schaltbild Single-Scart-Platine
Circuit diagram single scart board

Die Positionsnummern auf der Leiterplatte und dem Schaltbild sind mit der entsprechenden Vornummer zu ergänzen.

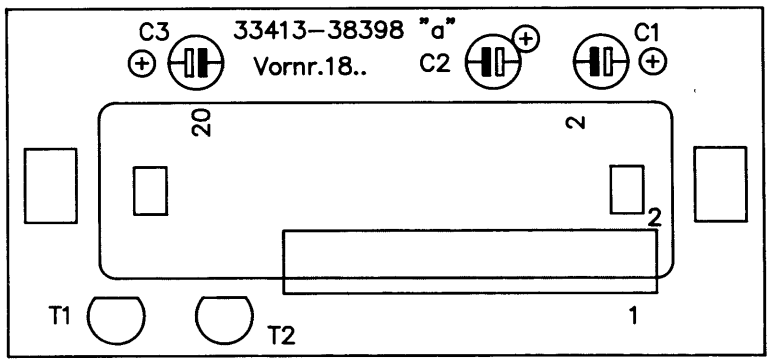
The position numbers on the P.C.B. and on the circuit diagram have to be completed with the corresponding key numbers.



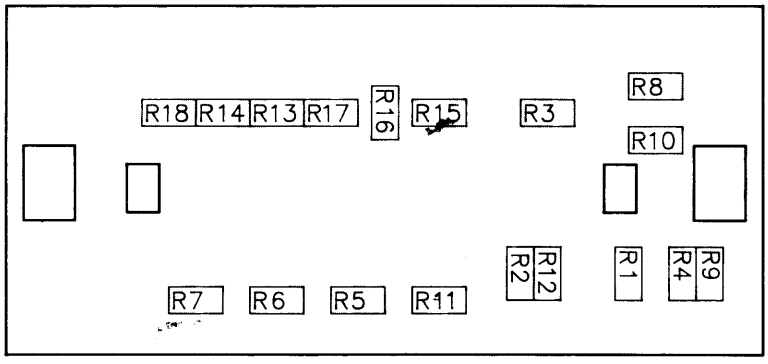
Single-Scart-Platine
Single Scart P.C.B.

Vornummer 18 . . .
Key number 18 . . .

Bestückungsseite
Top view



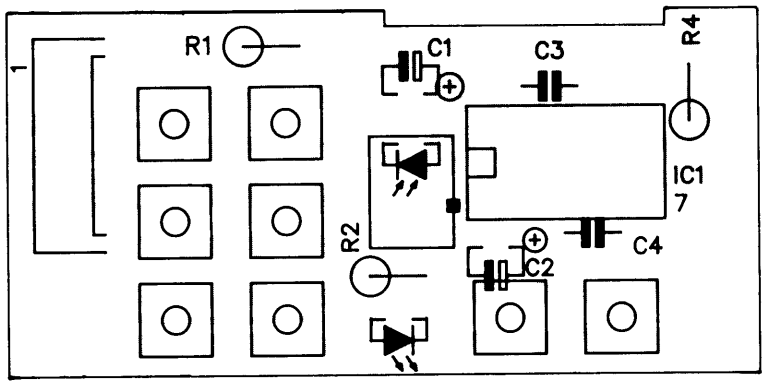
Chipseite
Chip view



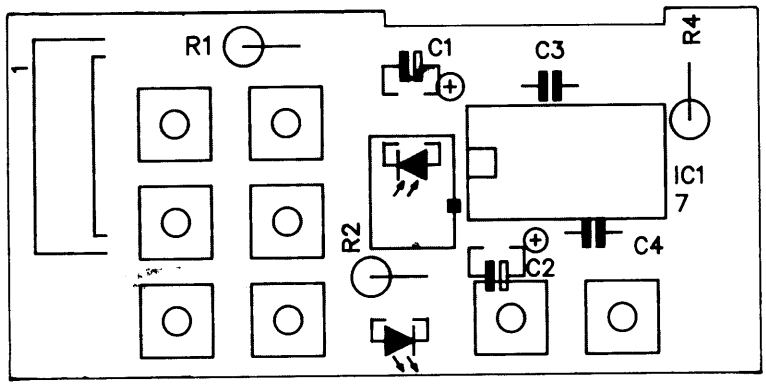
Bedienteilplatine Monitor
Control P.C.B. monitor

Vornummer 15 . . .
Key number 15 . . .

Bestückungsseite
Top view



Bestückungsseite und Leiterbahndarstellung Lötseite
Top view with layout soldering side



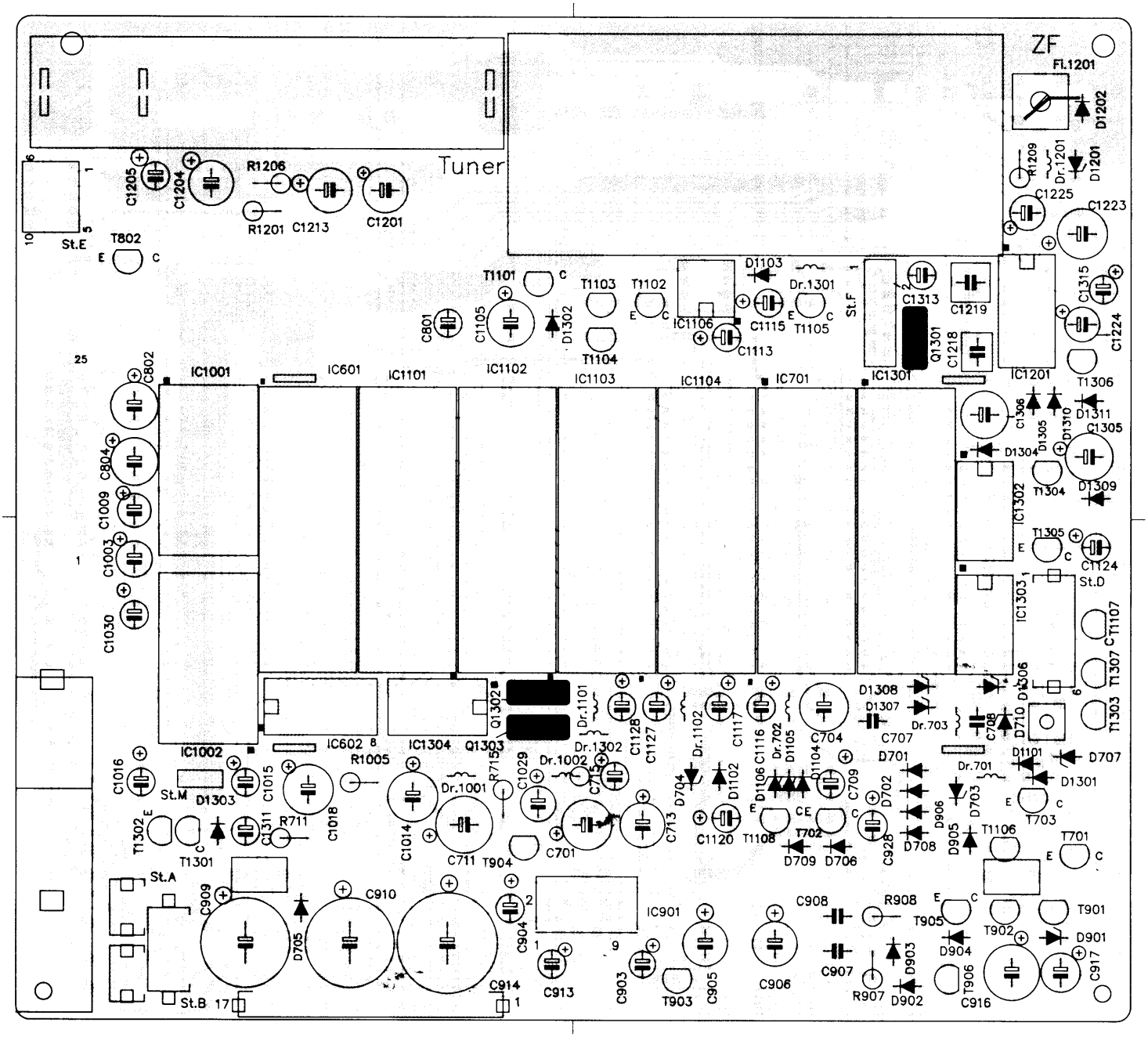
Signalteil

Signal unit P.C.B.

Vornummer 6, 7, 8, 9, 10, 11, 12, 13, 15 . . .
Key number 6, 7, 8, 9, 10, 11, 12, 13, 15 . . .

Bestückungsseite

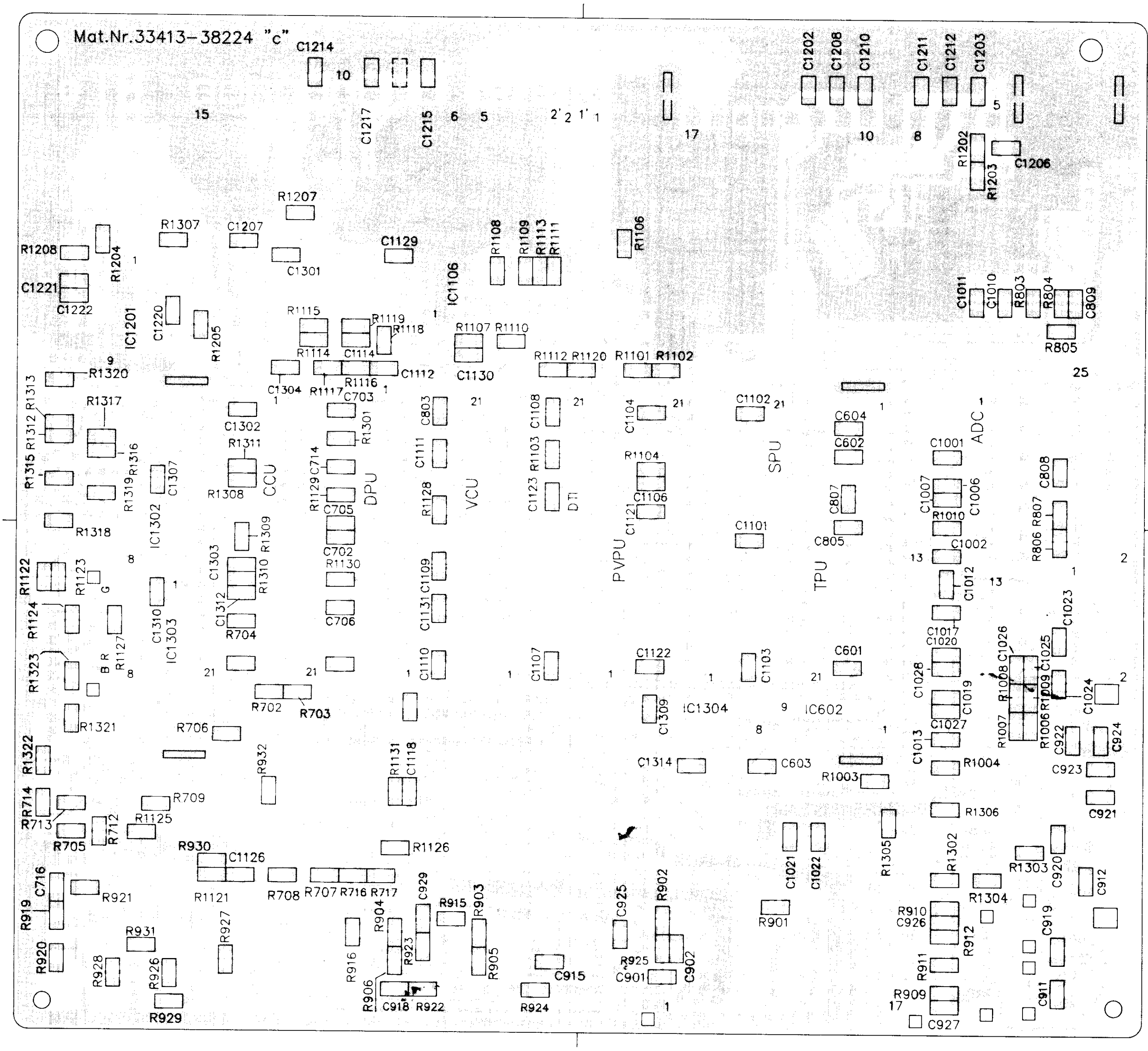
Top view



Signalteil
Signal unit P.C.B.

Vornummer 6, 7, 8, 9, 10, 11, 12, 13, 15 . . .
Key number 6, 7, 8, 9, 10, 11, 12, 13, 15 . . .

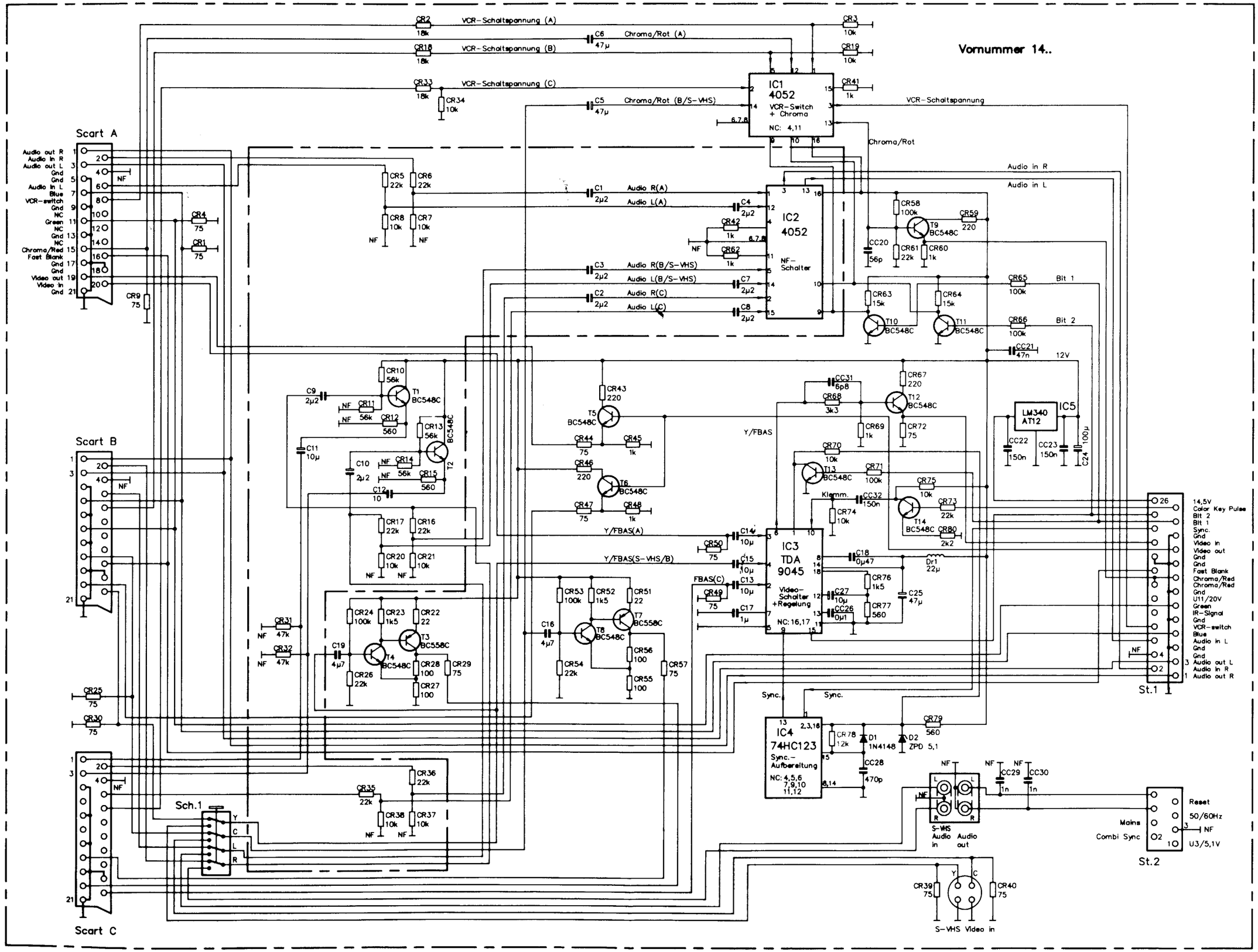
Chipseite
Bottom view



Schaltbild Multi-Scart
Circuit diagram multi-Scart

Die Positionsnummern auf der Leiterplatte und dem Schaltbild sind mit der entsprechenden Vornummer zu ergänzen.

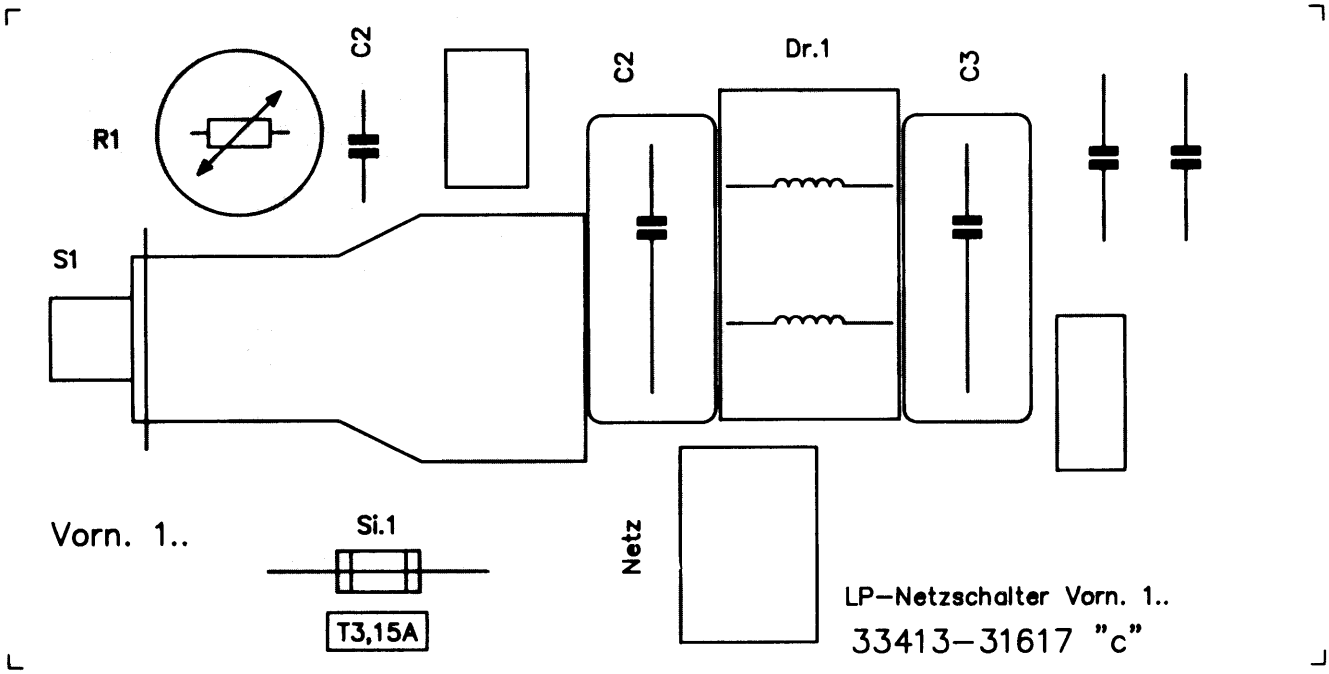
The position numbers on the P.C.B. and on the circuit diagram have to be completed with the corresponding key numbers.



Netzschalterplatine
Power switch P.C.B.

Vornummer 1 . . .
Key number 1 . . .

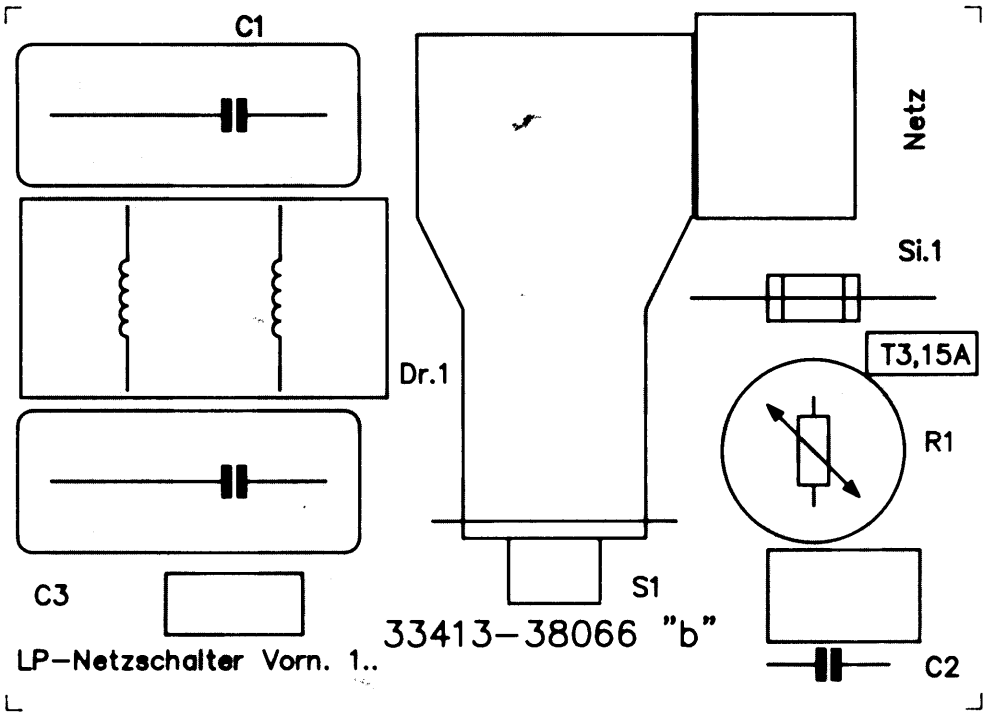
Bestückungsseite
Top view



Netzschalterplatine Monitor
Power switch P.C.B. monitor

Vornummer 1 . . .
Key number 1 . . .

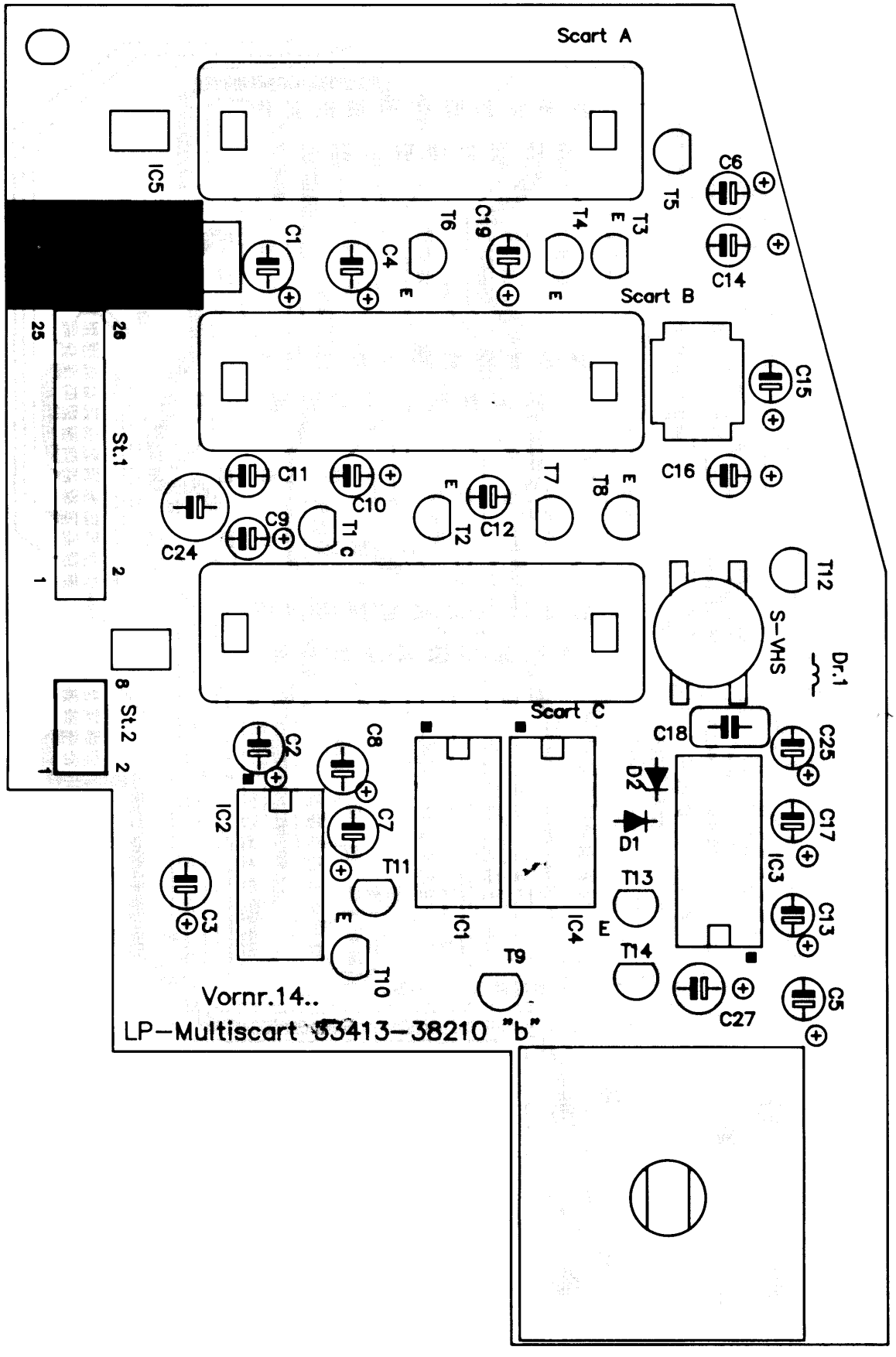
Bestückungsseite
Top view



Multi-Scart-Platine
Multi-Scart P.C.B.

Vornummer 14 . . .
Key number 14 . . .

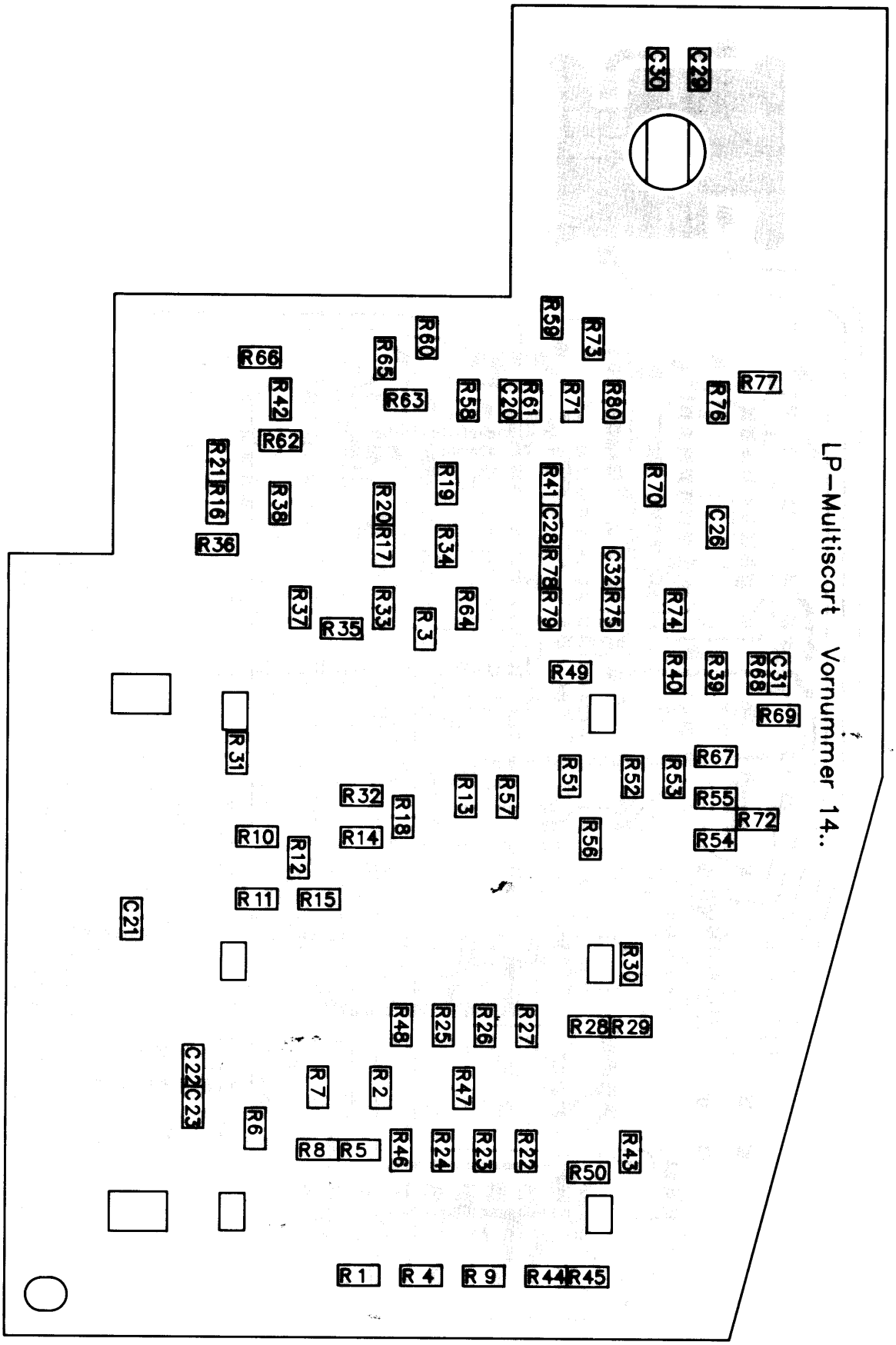
Bestückungsseite
Top view



Multi-Scart-Platine
Multi-Scart P.C.B.

Vornummer 14 . . .
Key number 14 . . .

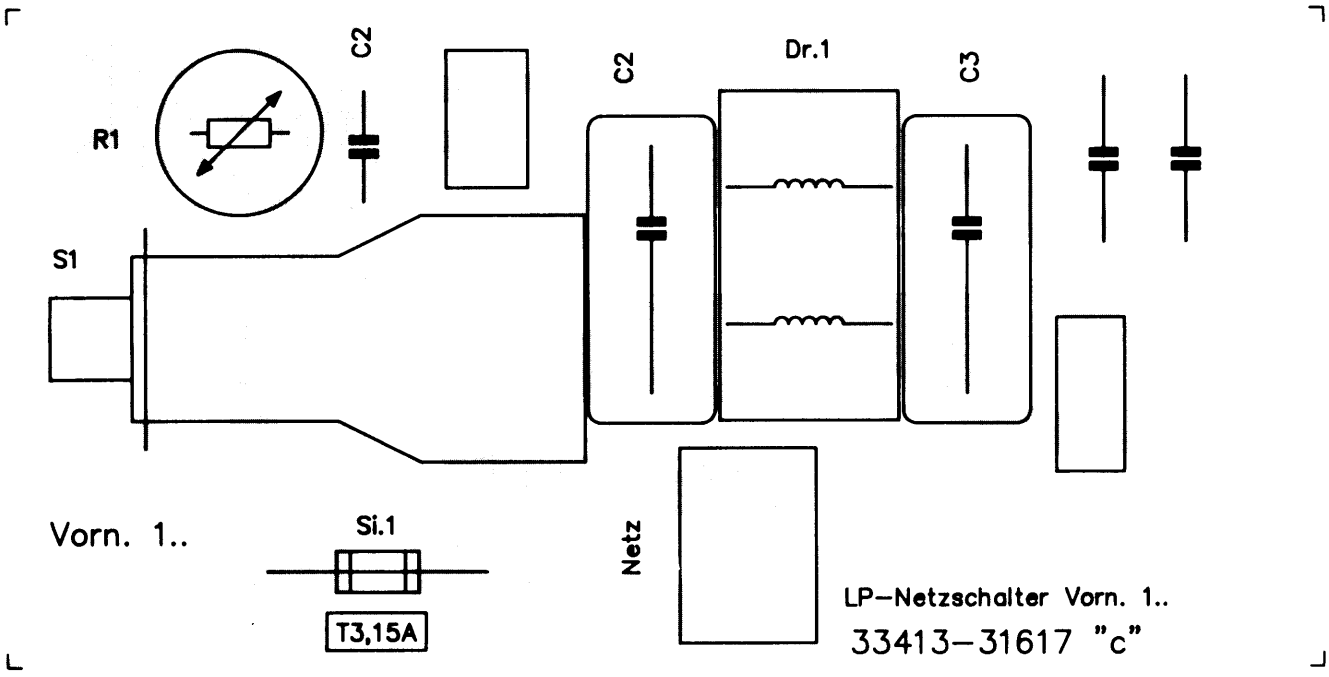
Leiterbahnseite
Bottom view



Netzschalterplatine
Power switch P.C.B.

Vornummer 1 . . .
Key number 1 . . .

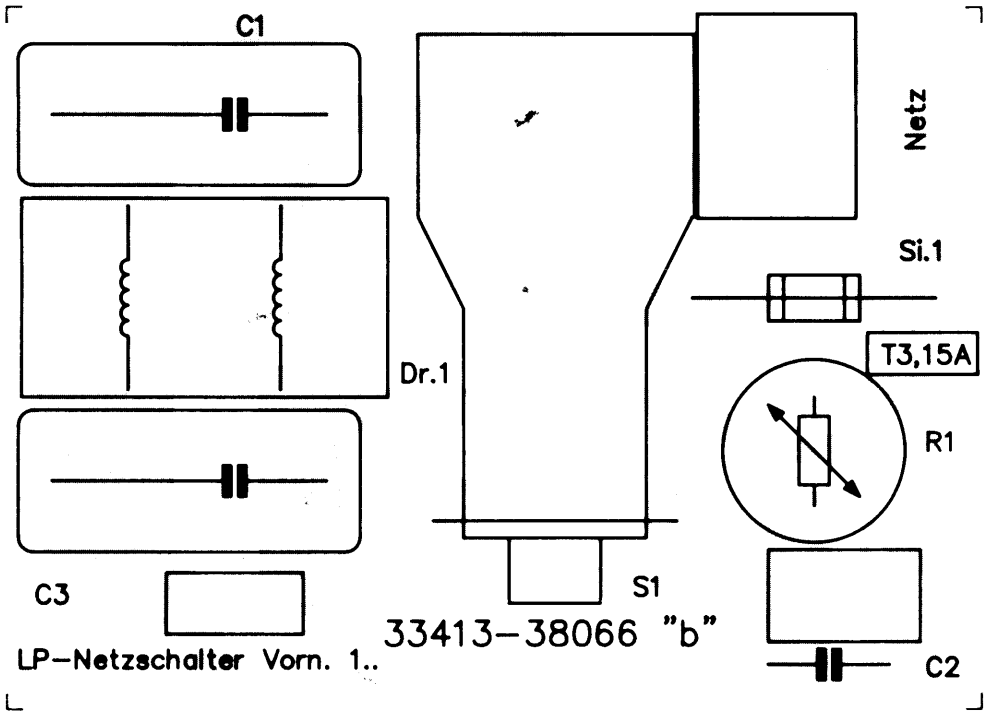
Bestückungsseite
Top view



Netzschalterplatine Monitor
Power switch P.C.B. monitor

Vornummer 1 . . .
Key number 1 . . .

Bestückungsseite
Top view



Ersatzteilliste Chassis
Spare parts list chassis

Achtung: Bestellhinweise (letzte Seite) beachten!
Important: Hints for order on last page!

Bestell-Nr./ Part. No.	Bezeichnung	Description	Position	Preisgruppe/ Price-key
	Signalteil-LP Chip	**Signal unit**	**B 1**	
38 477 00	IC CCU-S 7916	IC CCU-S 7916	IC 1301	C 6
38 478 00	IC MDA 2062-33	IC MDA 2062-33	IC 1302	B 4
38 479 00	IC MDA 2062-44	IC MDA 2062-44	IC 1303	B 4
31 612 00	IC TDA 2009	IC TDA 2009	IC 901	B 6
38 422 00	IC U 353 M	IC U 353 M	IC 1106	B 3
31 585 00	IC MCU 2600-53	IC MCU 2600-53	IC 1304	B 2
31 589 00	IC MEA 2901	IC MEA 2901	IC 1201	B 6
38 524 00	IC TPU 2732-01	IC TPU 2732-01	IC 601	D 6
31 627 00	IC 4164-15	IC 4164-15	IC 602	C 6
38 415 00	IC DPU 2553-01	IC DPU 2553-01	IC 701	C 6
38 416 00	IC VCU 2136-11	IC VCU 2136-11	IC 1104	C 2
38 417 00	IC DTI 2223-01	IC DTI 2223-01	IC 1103	B 8
38 418 00	IC PVPU 2204-02	IC PVPU 2204-02	IC 1102	C 3
38 419 00	IC APU 2471-01	IC APU 2471-01	IC 1002	C 6
38 420 00	IC ADC 2311-11	IC ADC 2311-11	IC 1001	B 6
38 421 00	IC SPU 2243-01	IC SPU 2243-01	IC 1101	C 3
23 964 00	Transistor BC 547 B	Transistor BC 547 B		A 4
31 849 00	Transistor BC 557 B	Transistor BC 557 B		A 1
31 318 00	Transistor BC 550	Transistor BC 550		A 1
31 995 00	Transistor BS 170	Transistor BS 170		B 7
31 463 00	Diode 1 N 4148	Diode 1 N 4148		A 1
31 811 00	Diode 1 N 4007	Diode 1 N 4007		A 2
31 317 00	Zenerdiode ZPD 5,6	Zenerdiode ZPD 5.6		A 1
31 384 00	Zenerdiode ZPD 30	Zenerdiode ZPD 30	D 1201	B 2
31 705 00	Diode ZPD 20	Diode ZPD 20	D 707	A 2
31 904 00	Zenerdiode ZPD 3,9	Zenerdiode ZPD 3.9	D 901	A 1
31 628 00	Quarz 14318,18 kHz	Crystal 14318.18 kHz	Q 1302	A 9
31 629 00	Quarz 17734,47 kHz	Crystal 17734.47 kHz	Q 1303	A 9
31 787 00	Quarz 4 MHz	Crystal 4 MHz	Q 1301	A 8
31 851 00	Sicherungs-Widerstand 12 R	Fuse resistor 12 R	R 715	A 2
31 851 00	Sicherungs-Widerstand 12 R	Fuse resistor 12 R	R 711	A 2
31 855 00	Sicherungs-Widerstand 4R7	Fuse resistor 4R7	R 1206	A 2
38 547 00	Sicherungs-Widerstand 22 R	Fuse resistor 22 R	R 1209	A 2
31 856 00	Sicherungs-Widerstand 56 R	Fuse resistor 56 R	R 1201	A 2
23 971 00	Drossel 22 µH	Coil 22 µH		A 2
31 902 00	Drossel 470 µH 1R7	Coil 470 µH	Dr. 1301	A 2
31 955 00	Drossel 4,7 µH R3	Coil 4.7 µH	Dr. 701/3	A 2
31 382 00	Zenerdiode ZPD 6,8	Zenerdiode ZPD 6.8		A 1
23 366 00	Taste Service	Button switch service		A 4
38 423 00	Tuner VHF/UHF/Hyperband	Tuner VHF/UHF/Hyperband		E 5
38 449 00	Rahmen-Ablenk/Signal	Frame	A 27	B 1
39 280 00	**ZF-Multinorm**	**IF multi standard**	**B 2**	**E 8**
02 432 00	Transistor BC 548 C	Transistor BC 548 C		A 1
31 810 00	Transistor BF 241	Transistor BF 241	MA-T 1705	A 2
31 831 00	IC TDA 4480	IC TDA 4480	IC 1701	C 4
31 463 00	Diode 1 N 4148	Diode 1 N 4148		A 1
31 832 00	Diode BA 282	Diode BA 282		A 1
31 833 00	Diode BB 609	Diode BB 609		A 1
14 580 00	Filter Keramik 5,5 MHz	Filter ceramic 5.5 MHz	Fi 1703	B 0
14 630 00	Filter Keramik 5,74 MHz	Filter ceramic 5.74 MHz	Fi 1704	B 0
31 701 00	Spule 38,9 MHz	Coil 38.9 MHz	L 1706	A 4
31 931 00	Spule 5,5/5,74 MHz TZF DEM	Coil 5.5/5.74 MHz	L 1701/02	A 8
31 923 00	Spule Q 120	Coil Q 120	L 1705	A 3
23 769 00	Filter BV 01 32,4 MHz ZF-BGL	Filter BV 01 32,4 MHz ZF-BGL	Fi 1703/04	A 3
31 891 00	Filter OFW L 9350	Filter OFW L 9350	Fi 1702	B 5
31 892 00	Filter OFW 6 3107	Filter OFW 6 3107	Fi 1701	B 5
38 458 00	Transistor BC 548 C	Transistor BC 548 C		A 1
31 810 00	Transistor BF 241	Transistor BF 241	T 1704	A 2
31 611 00	IC TDA 4453	IC TDA 4453	IC 1701	B 9
31 865 00	IC 74 HC 164	IC 74 HC 164	IC 1702	A 6
06 872 00	Zenerdiode ZPD	Zenerdiode ZPD	D 1706	A 1
31 463 00	Diode 1 N 4148	Diode 1 N 4148	D 1705	A 1
31 832 00	Diode BA 282	Diode BA 282		A 1
23 030 00	Filter F230 5,5 MA	Filter F230 5.5 MA	L 1702	A 5
31 829 00	Spule 38,9 MHz	Coil 38.9 MHz	L 1701	A 4
31 886 00	Filter OFW G 15	Filter OFW G 15	Fi 1701	C 2
31 921 00	Drossel 0,68 µH	Coil 0.68 µH	Dr. 1701	A 2
31 922 00	Keramik-Trap 4,5 MJ	Ceramic trap 4.5 MJ	Fi 1702	A 4
39 277 00	**ZF Standard B/G**	**IF standard B/G**	**B 2**	**E 0**
02 432 00	Transistor BC 548 C	Transistor BC 548 C	T 1702/03	A 3
10 797 00	Transistor BC 238 B	Transistor BC 238 B	T 1701	A 4
31 610 00	IC TDA 4445 A	IC TDA 4445 A	IC 1702	B 7
31 611 00	IC TDA 4453	IC TDA 4453	IC 1701	B 9
31 613 00	IC U 2829 B	IC U 2829 B	IC 1703	B 3
11 241 00	Diode 1 N 4148	Diode 1 N 4148	D 1701/02	A 2
31 828 00	Trimmpoti 22 K	Variable resistor 22 K	R 1719	A 2
31 906 00	Trimmpoti 2 K 2	Variable resistor 2 K 2	R 1702	A 2
14 580 00	Filter Keramik 5,5 MHz	Filter ceramic 5.5 MHz	Fi 1702	B 0
14 630 00	Filter Keramik 5,74 MHz	Filter ceramic 5.74 MHz	Fi 1703	B 0
23 030 00	Filter F230 5,5 MA MHz	Filter F 230 5.5 MA MHz	L 1705	A 5
31 700 00	Filter OFW G 3250	Filter OFW G 3250	Fi 1701	C 2
31 701 00	Spule 38,9 MHz	Coil 38.9 MHz	L 1701/02	A 4
31 703 00	Spule 5,5/5,74 MHz	Coil 5.5/5.74 MHz	L 1703/04	A 4

Ersatzteilliste Chassis
Spare parts list chassis

Achtung: Bestellhinweise (letzte Seite) beachten!

Important: Hints for order on last page!

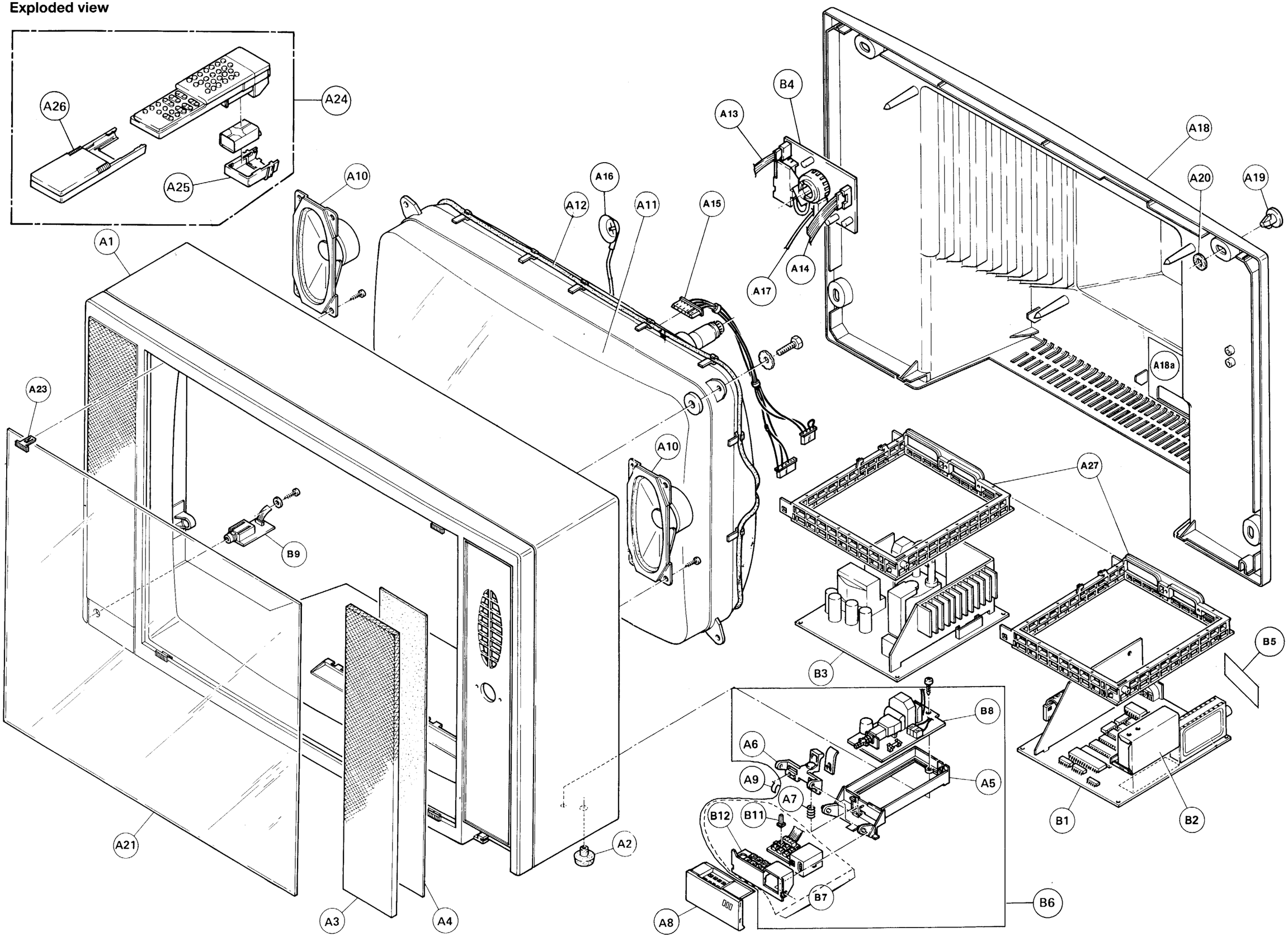
Bestell-Nr./ Part. No.	Bezeichnung	Description	Position	Preisgruppe/ Price-key
	Ablenkplatine	**Deflection unit**	**B 3**	
23 964 00	Transistor BC 547 B	Transistor BC 547 B		A 4
02 434 00	Transistor BC 558 B	Transistor BC 558 B		A 4
23 966 00	Transistor BC 416 C	Transistor BC 416 C	T 208/9	A 4
31 718 00	Transistor BC 639-10	Transistor BC 639-10	T 204/6	A 3
23 139 00	Transistor BU 508 A	Transistor BU 508 A	T 302	B 5
31 631 00	Transistor BD 683/DN 4359	Transistor BD 683/DN 4359	T 301/502	A 8
31 632 00	Transistor BD 202	Transistor BD 202	T 205	A 7
31 683 00	Transistor BU 801	Transistor BU 801	T 405	B 0
38 550 00	Transistor BUV 70	Transistor BUV 70	T 201	B 6
31 634 00	IC TEA 2164	IC TEA 2164	IC 201	B 6
31 684 00	IC LM 393 N	IC LM 393 N	IC 501/202	A 4
31 925 00	IC LM 317 T Stabi 1,25 V	IC LM 317 T Stabi 1.25 V	IC 203	A 9
38 540 00	IC L 7805 1,5 A/5,1 V 2%	IC L 7805 1.5 A/5.1 V 2%	IC 205	A 5
23 394 00	Diode EGP 20C 150/BYV 27/150	Diode EGP 20C 150/BYV 27/150	D 504/209	A 6
38 411 00	Diode BY 399	Diode BY 339	D 208	A 2
38 464 00	Diode BYW 80-50	Diode BYW 80-50	D 215	B 1
38 556 00	Diode BY 399	Diode BY 399	D 211	A 2
15 430 00	Gleichrichter B 250 C 2000/1500	Rectifier B 250 C 2000/1500	GL 201	A 8
31 729 00	Diode 1 N 4002	Diode 1 N 4002		A 2
23 951 00	Diode 1 N 4148	Diode 1 N 4148		A 2
31 719 00	Diode BA 157	Diode BA 157		A 1
31 720 00	Diode BA 159	Diode BA 159		A 2
31 384 00	Zenerdiode ZPD 30	Zenerdiode ZPD 30	D 218	A 2
31 630 00	Diode BY 228	Diode BY 228		A 2
31 809 00	Elko 1000 µF/25 V	Electrolyt capacitor 1000 µF/25 V	C 505	A 6
15 464 00	Elko 1000 µF/40 V	Electrolyt capacitor 1000 µF/40 V	C 214/215	A 7
31 808 00	Elko 220 µF/385 V	Electrolyt capacitor 220 µF/385 V	C 202	C 0
38 354 00	Elko 4700 µF/25 V	Electrolyt capacitor 4700 µF/25 V	C 218	B 2
38 615 00	Elko 10 µF/385 V	Electrolyt capacitor 10 µF/385 V	C 203	B 0
18 564 00	Kondensator 0,220 µF/ 250 V	Capacitor 0.220 µF/ 250 V	C 201	A 7
18 633 00	Kondensator 0,011 µF/1600 V	Capacitor 0.011 µF/1600 V	C 304	A 7
31 742 00	Kondensator 6800 pF/1000 V	Capacitor 6800 pF/1000 V	C 305	A 4
31 745 00	Kondensator 1000 pF/1600 V	Capacitor 1000 pF/1600 V	C 307	A 4
31 746 00	Kondensator 1200 pF/1600 V	Capacitor 1200 pF/1600 V	C 308	A 4
31 749 00	Kondensator 3,300 µF/160 V	Capacitor 3.300 µF/160 V	C 507	B 2
38 016 00	Kondensator 0,22 µF/250 V	Capacitor 0.22 µF/250 V	C 309/310	A 5
38 033 00	Kondensator 1200 pF/400 V	Capacitor 1200 pF/400 V	C 508	A 4
38 400 00	Kondensator 2,2 nF/1600 V	Capacitor 2.2 nF/1600 V	C 209	A 4
23 317 00	Kondensator 2,2 nF/4 kV	Capacitor 2.2 nF/4 kV	C 210	A 7
23 131 00	Widerstand 2R2/½ W	Resistor 2R2/½ W	R 409	A 1
31 853 00	Widerstand 1R5/½ W	Resistor 1R5/½ W	R 519	A 1
15 443 00	Widerstand 51R/½ W	Resistor 51R/½ W	R 305/520	A 1
31 822 00	Widerstand 33K/½ W	Resistor 33K/½ W	R 201	A 0
38 146 00	Widerstand 150R/½ W	Resistor 150R/½ W	R 242	A 0
38 549 00	Widerstand 0,24/1 W	Resistor 0.24/1 W	R 216	A 1
38 404 00	Widerstand 220R/1 W	Resistor 220R/1 W	R 215	A 3
38 412 00	Widerstand 1R/1 W	Resistor 1R/1 W	R 230	A 3
38 413 00	Widerstand 47R/1 W	Resistor 47R/1 W	R 302	A 3
38 414 00	Widerstand 56K/1 W	Resistor 56K/1 W	R 223	A 3
38 315 00	NTC-Widerstand 100 R	NTC resistor 100 R	R 521	A 4
18 626 00	Sicherungswiderstand 1K	Fuse resistor 1K	R 307/R 518	A 3
23 056 00	Sicherungswiderstand 4R7	Fuse resistor 4R7	R 308, 413, 517	A 2
23 291 00	Sicherungswiderstand 0,47	Fuse resistor 0.47	R 303	A 7
31 823 00	Sicherungswiderstand 220R	Fuse resistor 220R	R 516	A 7
38 474 00	Sicherungswiderstand 22R	Fuse resistor 22R	R 412	A 2
31 146 00	Widerstand 10M	Resistor 10M	R 217	A 1
23 295 00	Trimmpoti 5K	Variable resistor 5K	R 226	A 2
31 691 00	Trafo Treiber horizontal	Transformer horiz. drive	TR 301	B 0
31 692 00	Trafo Dioden-Split	Transformer diode split	TR 302	D 3
38 391 00	Trafo Netzteil	Transformer switch mode	TR 202	C 7
38 392 00	Trafo Trigger	Transformer trigger	TR 201	B 1
15 481 00	Spule Linearität	Coil linearity	DR 301	B 0
31 908 00	Spule vert. 360 µH	Coil vert. 360 µH	DR 501	B 2
38 406 00	Netz-Drossel 2 × 33 mH	Line filter 2 × 33 mH	DR 201	B 3
23 861 00	Drossel 180 µH	Coil 180 µH	DR 202	A 8
31 902 00	Drossel 470 µH	Coil 470 µH	DR 204	A 2
31 955 00	Drossel 4,7 µH	Coil 4.7 µH	DR 203	A 2
38 568 00	Montageclip	Clip	D 215	A 1
31 331 00	Montageclip TO 220	Clip TO 220		A 0
23 072 00	Montageclip SOT 82	Clip SOT 82		A 2
15 427 00	Montageclip SOT 93	Clip SOT 93		A 1
38 449 00	Rahmen-Ablenk/Signal	Frame signal unit	A 27	B 1
38 052 00	Clip Anodenleitung	Clip anode cable		A 0
38 053 00	Clip Focusleitung	Clip focus cable		A 0
39 241 00	**Single-Scart-Platine**	**Single Scart board**	**B 5**	
23 964 00	Transistor BC 547	Transistor BC 547	T 1801, 1802	A 4
38 189 00	Scart-Buchse	Scart jack		B 0

Ersatzteilliste Chassis
Spare parts list chassis

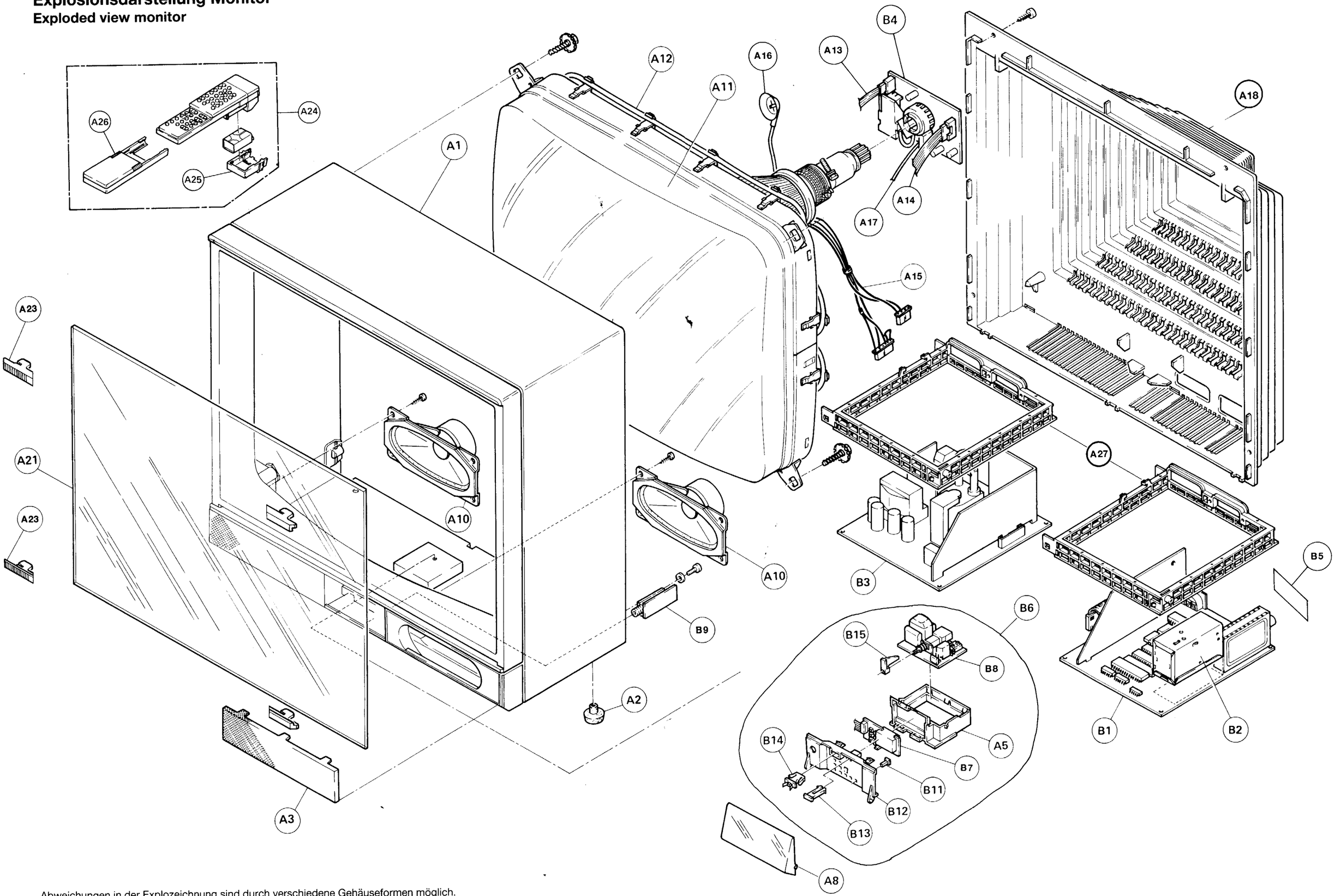
Achtung: Bestellhinweise (letzte Seite) beachten!
Important: Hints for order on last page!

Bestell-Nr./ Part. No.	Bezeichnung	Description	Position	Preisgruppe/ Price-key
39 121 00	**Multi-Scart-Platine**	**Multi Scart board**	**B 5**	**E 3**
38 458 00	Transistor BC 548 C	Transistor BC 548 C	div.	A 1
06 052 00	Transistor BC 558 B	Transistor BC 558 B	T 1403, 1407	A 5
38 470 00	Transistor BS 107	Transistor BS 107	T 1414	A 3
31 817 00	IC LM 340 T 12	IC LM 340 T 12	IC 1405	A 5
38 211 00	IC HEF 4052 B	IC HEF 4052 B	IC 1401/1402	A 4
38 212 00	IC TDA 9045	IC TDA 9045	IC 1403	C 3
38 213 00	IC 74 HC 123	IC 74 HC 123	IC 1404	A 5
06 872 00	Zenerdiode ZPD 5,1	Zenerdiode ZPD 5.1	D 1402	A 1
31 463 00	Diode 1 N 4148	Diode 1 N 4148	D 1401	A 1
23 059 00	Drossel 22 µH	Coil 22 µH	Dr. 1401	A 4
18 549 00	Druckschalter	Push switch	S 1401	B 1
38 317 00	Tastenknopf ∅=10 mm	Knob ∅=10 mm		A 4
38 189 00	Scart-Buchse 21pol.	Scart jack 21-pin		B 0
38 190 00	Chinch-Buchse 4fach	Chinch jack 4 ×		B 1
38 316 00	S-VHS-Buchse 4pol.	Jack S-VHS 4-pin		A 8
39 274 00	**Bildrohrplatine Full/Pill**	**Picture tube board Full/Pill**	**B 4**	**D 8**
39 273 00	**Bildrohrplatine Flat**	**Picture tube board Flat**	**B 4**	**D 8**
23 058 00	Transistor BF 871	Transistor BF 871	T 1602-06-10	A 4
23 964 00	Transistor BC 547 B	Transistor BC 547 B	T 1613	A 4
23 965 00	Transistor BC 558 B	Transistor BC 558 B	T 1601-05-09-14	A 4
31 676 00	Transistor BF 422 S	Transistor BF 422 S	T 1603-07-11-15	A 2
38 319 00	Transistor BF 421 S	Transistor BF 421 S	T 1604-08-12	A 2
23 951 00	Diode 1 N 4148	Diode 1 N 4148		A 2
31 729 00	Diode 1 N 4002	Diode 1 N 4002		A 2
31 811 00	Diode 1 N 4007	Diode 1 N 4007		A 2
06 055 00	Zenerdiode ZPD 15	Zenerdiode ZPD 15	D 1610	A 2
31 902 00	Drossel 470 µH	Coil 470 µH	Dr. 1634	A 2
31 793 00	Kondensator 0,022 µF/1500 V	Capacitor 0.022 µF/1500 V	C 1613	
31 857 00	Sicherungswiderstand 1 K	Fuse resistor 1 K	R 1608-15-22	A 2
31 856 00	Sicherungswiderstand 56R	Fuse resistor 56R	R 1637	A 2
31 727 00	Widerstand 1K	Resistor 1K	R 1609-16-23-36	A 0
11 383 00	Trimmpoti 470R	Variable resistor 470R	R 1627	A 3
18 206 00	Clip Focusleitung	Clip focus cable		A 0
31 997 00	Focus UG 2-Poti Full/Pil	Variable resistor focus/UG 2 Full/Pil		B 9
31 666 00	Focus UG 2-Poti Flat	Variable resistor focus/UG 2 Flat		B 9
18 645 00	Röhrensockel 8pol. Full/Pil	Socket picture tube Full/Pil		B 4
31 052 00	Röhrensockel 8pol. Flat	Socket picture tube Flat		B 4
39 286 00	**Netzschalterplatine**	**Power switch board**	**B 8**	
39 287 00	**Netzschalterplatine Monitor**	**Power switch board monitor**	**B 8**	
15 433 00	Widerstand PTC	Resistor PTC	R 101	A 8
38 406 00	Netz-Drossel 2 × 33 mH	Line filter 2 × 33 mH	Dr. 101	B 4
31 743 00	Netzschalter	Power switch	S 1010	B 2
20 944 00	**Bedienteilplatine**	**Control board**	**B 7**	**D 5**
39 079 00	**Bedienteilplatine Monitor**	**Control board monitor**	**B 7**	**D 5**
31 588 00	IC TBA 2800	IC TBA 2800	IC 1501	B 1
31 905 00	IR-Diode Empfang	IR diode remote	D 1501	A 8
38 186 00	Leuchtdiode grün Monitor	LED green monitor		A 3

Explosionsdarstellung
Exploded view



Explosionsdarstellung Monitor
Exploded view monitor



Abweichungen in der Explozeichnung sind durch verschiedene Gehäuseformen möglich.
Some differences in the exploded view are possible to the consisted unit.

Ersatzteilliste Explo
Spare parts list explo

Achtung: Bestellhinweise (letzte Seite) beachten!

Important: Hints for order on last page!

Bestell-Nr./ Part. No.		Bezeichnung	Description	Position	Preisgruppe/ Price-key
	5	Gehäuse kpl.	Housing complete	A 1	F 5
		Gehäusefuß	Housing foot	A 2	A 1
		Abdeckgitter rechts	Mask right	A 3	C 7
		Abdeckgitter links	Mask left	A 3	C 7
		Schaumstoff-Einlage	Inserted cover	A 4	A 7
		Rahmen-Netzteil	Frame power supply	A 5	B 0
		Bügel	Bow	A 6	A 3
		Druckfeder	Pressure spring	A 7	A 0
	20.	Blende-Bed. —	Mask	A 8	B 9
		Feder für Klappe	Spring	A 9	A 3
	20	Lautsprecher	Speaker	A 10	C 7
		Farbbildröhre	Picture tube	A 11	
	5	Entmagnetisierungsspule	Demagnetizing coil	A 12	C 4
31 753 00		Bandleitung 4 × 0,5/440 mm	Ribbon cable 4 × 0.5/440 mm	A 13	A 8
31 679 00		Bandleitung 6 × 0,5/430 mm	Ribbon cable 6 × 0.5/430 mm	A 14	A 9
		Kabelbaum Ablenkspulen	Wiring deflection coil	A 15	B 1
31 834 00		Hochspannungsleitung	High-voltage cable	A 16	B 2
31 835 00		Focusleitung	Focus cable	A 17	A 5
	5	Rückwand	Back cover	A 18	D 5
	5	Blende Rückwand	Panel back cover	A 18a	B 2
		Befestigungsknebel	Toggle back cover	A 19	A 2
		Gummiring	Rubber ring	A 20	A 0
		Frontscheibe	Glass	A 21	
	~~30~~	Scheibenhalter	Holder glass	A 23	A 2
	20	Fernbedienungsgeber	Remote control	A 24	D 8
	30	Batteriefachdeckel	Cover battery	A 25	A 9
	20	Schubabdeckung, Geber	Slide cover, remote control	A 26	B 8
		Rahmen Chassis	Frame chassis	A 27	B 1
	10	Signalplatine	Signal unit	B 1	
		ZF-Platine	IF board	B 2	
31 783 00		ZF-Abschirmbecher	IF shielding	B 2	B 2
	10	Ablenkplatine	Deflection unit	B 3	
	—	Bildrohrplatine	Picture tube board	B 4	
		Single-Scart-Platine	Single Scart board	B 5	
		Multi-Scart-Platine	Multi Scart board	B 5	
	[redacted]	Bedienteil/Netzschalter-Platine kompl.	Control/power switch assembly	B 6	
	[redacted]	Bedienteilplatine	Control board	B 7	
	20	Netzschalterplatine	Power switch board	B 8	
	20	Kopfhörerbuchse	Headphone jack	B 9	A 9

IDENT No. 49028

B13
B14

20. Ribbon cable to suit B1 to B7
(Signal to Remote P.C.B.)

Bestellhinweise:
Hints for order:

Bitte bei Ersatzteilbestellung die genaue Bezeichnung und **Ident-Nr. (siehe Typenschild)** des Gerätes sowie Bestell-Nummer und Positions-Nummer des Ersatzteils angeben.
Bei Ersatzteilen ohne Bestellnummer sind unbedingt die Ident-Nummer (siehe Typenschild auf Geräterückseite) und die Positionsnummer (Explo) bzw. die Positionsnummer mit Vornummer aus dem Schaltbild erforderlich.

For ordering of spare parts please state exact description and **ident no. of unit (see silver rating label on the backside of unit)** as well as part no. and position no. of required spare parts.
Spare parts without order number, the ident number (silver label on backside) and the position number (explo) respectively the position number with key number (circuit diagram) is absolutely necessary.

Bei Einsendung bitte folgendes beachten:

Farbbildröhre ist mit den Ablenkspulen eine Einheit.
Entmagnetisierungsspule mit Halter, Masseband und Anschlußleitungen für Ablenkspulen nicht einsenden!

Ablenkchassis mit Kunststoffrahmen einsenden. Focusleitung, Anodenleitung und andere steckbare Verbindungsleitungen nicht einsenden!

Signalchassis mit Kunststoffrahmen und Tuner einsenden.
ZF-Platine und steckbare Verbindungsleitungen nicht einsenden!

By return please attention following:

Color picture tube is a unit with the deflection coils.
Degausing coil with holder, ground wiring and wiring for deflection coils don't send.

Deflection unit send with frame. Focus cable, anode cable and other connectors don't send.

Signal unit send with frame and tuner.
IF board and other connectors don't send.

Benutzen Sie:

Telex: 531516

oder

Bildschirmtext *317298 #

oder

Telefax: 08245/51326

Änderungen vorbehalten.
Modifications reserved.

Schulungs Unterlagen

DTV 2

Schneider

Inhaltsverzeichnis

CCU 2030,
CCU 2050, CCU 2070
Central Control Units

2. Features of the CCU 2030, CCU 2050 and CCU 2070 Central Control Units

All three types, differing only in their ROM and RAM capacity, are the unprogrammed versions and are programmed during production according to the customer's specifications. For programming, an emulator board is available. The programmed versions have the type designations CCU 2031, CCU 2032 and so on. Combined with peripheral hardware, CCU 2030, CCU 2050 and CCU 2070 offer the following features:

- infrared remote control
- front-panel control with up to 32 commands
- tuning by frequency synthesis (PLL) and band switching
- non-volatile program storage
- LED display for channel indication, max. 4 digits, directly driven
- storage of alignment information during production
- generation and recognition of various signals
- control of the digital signal processors for video, audio, teletext and deflection via a serial bus (IM bus)

The CCUs are produced in N-channel HMOS technology, are housed in a 40-pin Dil plastic package, and contain on one chip the following functions (Fig. 4):

- 8049 8-bit microcomputer
- remote-control decoder
- Ports P2 and P3 for connecting a maximum of 32 keys and 4-digit seven-segment LED channel indication
- PLL tuner circuit for VHF and UHF
- IM bus interface for inputting and outputting control signals and for inputting alignment instructions
- crystal-controlled clock oscillator which also serves as reference for the PLL circuit
- mains flip-flop and reset circuit

This specification is restricted to the hardware aspects of the CCU 20.0 Central Control Unit. Many functions are defined in detail by the microcomputer's ROM code and are thus described in the program specifications of the individual applications. For understanding the operation of the CCU, the following texts are useful: IM bus specification (section 11.) and the manual of the 48-series microprocessor family (see sections 12. and 13.).

3. Functional Description

The CCU 20.0 Central Control Unit provides an efficient interface between user and TV set. Their programmability enables different set makers to design receivers according to their own specs. The CCU has the main functions:

- processing of user's settings
- control of the digital signal processors for video, audio, Teletext and deflection

By means of the MDA 2062 non-volatile memory (EEPROM) which has a capacity of 128 × 8 bits, the CCU controls storage and output of factory alignment values that have been programmed during production of the TV set.

3.1. User's settings

All user settings such as channel selection, station search, adjustment of volume, brightness, color saturation, etc. are fed to the CCU either by infrared remote control or by means of the local keyboard (direct input, up to 32 keys).

The tuning system is designed as a frequency synthesizer using a PLL with a resolution of 62.5 kHz. It requires a predivider with a fixed ratio of 64:1. Station keys can be programmed for selected channels, the tuning information being stored in the MDA 2062 EEPROM.

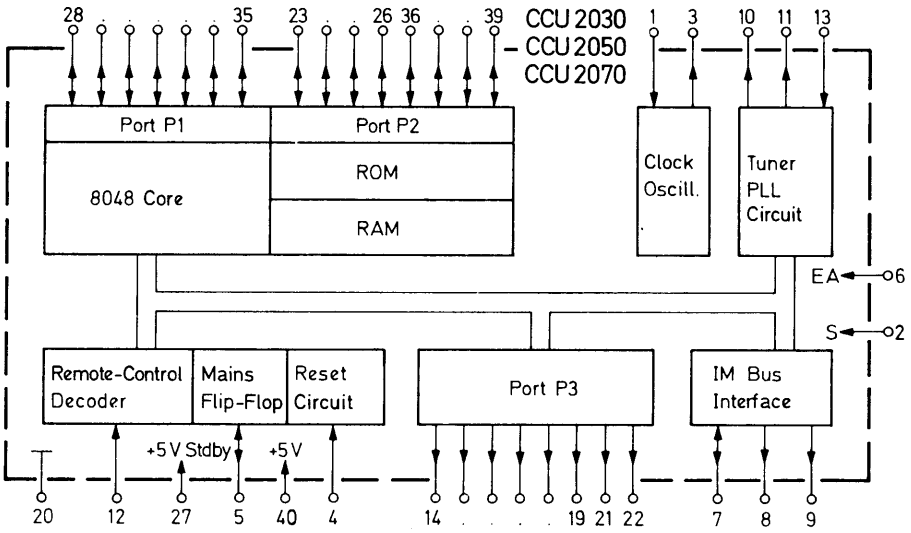


Fig. 4: Block circuit diagram of the CCU 2030/CCU 2050/CCU 2070

10. Description of the Connections and Signals

Pin 1 – XTAL: Oscillator Crystal
The internal configuration of this in/output is shown in Fig. 8. For normal use, a 4 MHz crystal is connected to this oscillator pin and to GND. The input is self-biasing to approx. 3.5 V, input DC resistance is approx. 350 kΩ. The output signal is the 4 MHz clock signal of the CCU. It may be fed to other circuits, but maximum load configurations have to be observed as loading affects oscillation start-up after power-on of the ST.BY supply (see section 8.).

Pin 2 – S: Single-Step Input
The internal configuration of this input is shown in Fig. 9. Via this input, the CCU can be put into the single-step mode (see section 12.2.2.). The inactive low level is 0 to +5 V and the required, active high level is +12 V. The input contains a pull-down device (about 30 µA to GND) which allows to leave the input unconnected for normal operation.

Pin 3 – Osc Out: $f_{osc}/4096$ Output
The internal configuration of this output is shown in Fig. 10. This output provides the memory clock signal for the MDA 2062 EEPROM (1 kHz). The drive capability of pin 3 is one TTL gate. The frequency is selected by a mask option (see section 14.).

Pin 4 – $\overline{\text{Reset}}$: Reset Input
The internal configuration of this input is shown in Fig. 11. An active low level at this pin provides normalization for µC and peripheral circuits. An inactive high level is fed to the µC and peripheral circuits depending on the state of the mains flip-flop and the setting of the reset options (cf. sections 4.6. and 14.). The input circuit is of a Schmitt trigger configuration and provides some noise immunity. In critical applications, however, an additional ceramic capacitor, connected between this pin and GND, may be necessary to increase noise immunity.

Pin 5 – $\overline{\text{Mains}}$: Mains Switch Input/Output
The internal configuration of this in/output is shown in Fig. 12. Pin 5 represents the output of the mains flip-flop with a resistive pull-up. The output is active low (mains on). By shorting this pin to GND momentarily, the mains flip-flop is set to the active, low state via the input circuitry of this pin. The resistive pull-up provides drive for a PNP transistor connected emitter to ST.BY, base via a resistor to pin 5, and collector to the mains relay. A detailed functional description of the mains flip-flop and reset circuit is given in section 4.6.

Pin 6 – EA: Test Enable Input
The internal configuration of this input is shown in Fig. 9. Pin 6 is a test input providing external access to the µC (cf. sections 5. and 12.2.4.). For normal operation, an inactive low level is required at this pin (GND).

Pin 7 to 9 – Data, Ident, Clock: IM Bus Connections
The internal configurations of these pins are shown in Figs. 12 and 13. By means of these pins, the CCU links with peripheral devices. The IM bus is described in detail in section 11. Please note that the resistive pull-ups for all open-drain outputs connected to the IM bus are situated within the CCU.

Pins 10 and 11 – Up and Down: Tuning Voltage Outputs
The internal configuration of these pins is shown in Fig. 13. Active high levels on these outputs indicate whether the tuner frequency should be increased (Up) or reduced (Down) and represent the output signals of the phase-locked loop circuit of the CCU (cf. section 4.4.). The outputs contain resistive pull-ups.

Pin 12 – IR: Remote-Control Input
The internal configuration of this pin is shown in Fig. 14. Via an external coupling capacitor of 10 nF, the remote-control signal, amplified by the TBA 2800 preamplifier IC, is fed to the remote-control decoder contained in the CCU (cf. section 4.2.). The input is self-biasing to approx. 1.4 V, and the input DC resistance is approx. 150 kΩ. For highest input sensitivity, this pin must not be loaded resistively.

Pin 13 – LO: Local Oscillator Input
The internal configuration of this input is shown in Fig. 14. Via an external coupling capacitor of at least 1 nF, the tuner oscillator frequency (signal), divided by 64 by a prescaler device, is fed to the PLL circuit contained in the CCU, thereby providing feedback from the tuner oscillator (cf. section 4.4.). The input is self-biasing to approx. 1.7 V, and the input DC resistance is approx. 200 kΩ. For highest input sensitivity, this pin must not be loaded resistively.

Pin 14 to 19, 21 and 22 – Port P3, Bits 0 to 7
The internal configuration of these outputs or test in/outputs is shown in Fig. 15. During normal use, these open-drain outputs provide multiplexed drive for LED display and keyboard (cf. section 4.3.). The voltage handling capability is limited to V_{DD}. During test operations (EA at or above 5 V, cf. section 5.), these pins give access to the µC bus port DB_0 to DB_7 which also connects to peripheral circuits as PLL, IM bus interface, remote-control decoder etc. Drive capability of the bus port via P3 is very limited (external CMOS bidirectional buffers required).

Pin 20 – GND: Ground, 0
This pin must be connected to the negative of the supply. It may also be designated V_{SS}. Please note that current on this pin is total V_{DD} and ST.BY supply current plus currents flowing into outputs (Port P3) and may amount to more than 300 mA.

Pins 23 to 26 and 36 to 39 – Port P2, Bits 0 to 7
The internal configuration of these in/outputs or test outputs is shown in Fig. 16. Direct data transfer with the µC can be executed via this port (cf. sections 12.2.12. and 4.3.). The outputs drive one TTL gate. Open-drain outputs with a 5 V rating may be specified on each single pin of this port as an option (cf. section 14.). During test operations (EA at or above 5 V, cf. section 5.), $P2_4$ to $P2_7$ give access to the µC output signals $\overline{\text{RD}}$, $\overline{\text{WR}}$, ALE and $\overline{\text{PSEN}}$ which also connect to peripheral circuits as PLL, IM bus interface, remote-control decoder etc. Drive capability of the µC control signals via connections $P2_4$ to $P2_7$ is very limited (external CMOS buffers required).

Pin 27 – ST.BY: Standby Supply Voltage
This pin must be connected to the positive of the 5 V standby supply. It powers the crystal oscillator, the mains flip-flop and reset circuits, the remote-control decoder and a specific portion of the µC-resident RAM. From standby operation, an infrared signal may activate the mains flip-flop and thus awake the system to full operation.

Pins 28 to 35 – Port P1, Bits 0 to 7
The internal configuration of these in/outputs is shown in Fig. 17. Direct data transfer with the µC can be executed via this port (cf. section 12.2.12.). The outputs are open-drain with a 12 V rating.

Pin 40 – V_{DD}: Supply Voltage
This pin must be connected to the positive of the 5 V supply.

11. Description of the IM Bus

The INTERMETALL Bus (IM Bus for short) has been designed to control the DIGIT 2000 ICs by the CCU Central Control Unit. Via this bus the CCU can write data to the ICs or read data from them. This means the CCU acts as a master whereas all controlled ICs are slaves.

The IM Bus consists of three lines for the signals Ident (ID), Clock (CL) and Data (D). The clock frequency range is 50 Hz to 170 kHz. Ident and clock are unidirectional from the CCU to the slave ICs, Data is bidirectional. Bidirectionality is achieved by using open-drain outputs with On-resistances of 150 Ω maximum. The 2.5 kΩ pull-up resistor common to all outputs is incorporated in the CCU.

The timing of a complete IM Bus transaction is shown in Fig. 18 and Table 1. In the non-operative state the signals of all three bus lines are High. To start a transaction the CCU sets the ID signal to Low level, indicating an address transmission, and sets the CL signal to Low level as well to switch the first bit on the Data line. Thereafter eight address bits are transmitted beginning with the LSB. Data takeover in the slave ICs occurs at the High levels of the clock signal. At the end of the address byte the ID signal goes High, initiating the address comparison in the slave circuits. In the addressed slave the IM bus interface switches over to Data read or write, because these functions are correlated to the address.

Also controlled by the address the CCU now transmits eight or sixteen clock pulses, and accordingly one or two bytes of data are written into the addressed IC or read out from it, beginning with the LSB.

The Low clock level after the last clock pulse switches the Data line to High level. After this the completion of the bus transaction is signalled by a short Low-state pulse of the ID signal. This initiates the storing of the transferred data.

It is permissible to interrupt a bus transaction for up to 10 ms.

For future software compatibility, the CCU must write a zero into all bits not used at present. When reading undefined or unused bits, the CCU must adopt "don't care" behaviour.

Table 1: Timing of the IM bus signals

Time	t_{IM1}	t_{IM2}	t_{IM3}	t_{IM4}	t_{IM5}	t_{IM6}	t_{IM7}	t_{IM8}	t_{IM9}	t_{IM10}
Min. µs	0	3.0	3.0	0	1.5	6.0	0	0	0	3.0

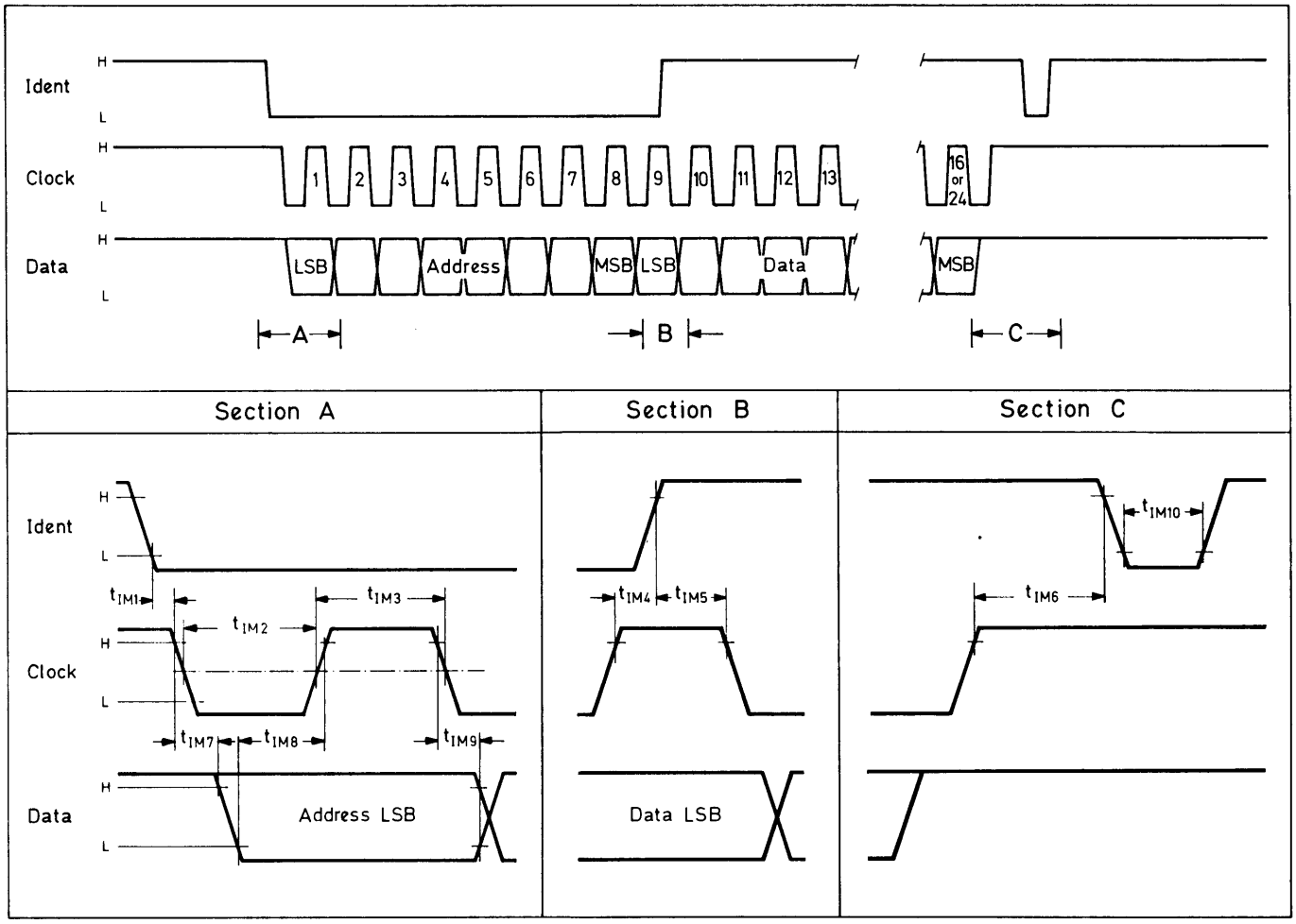
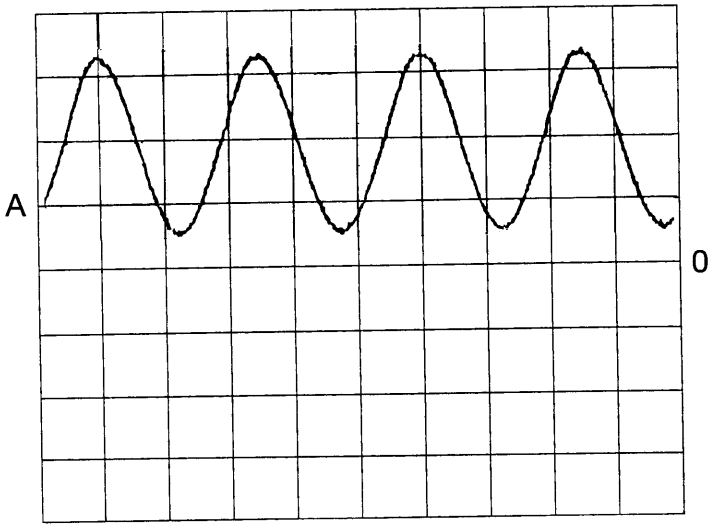


Fig. 18: Waveforms of the IM bus signals

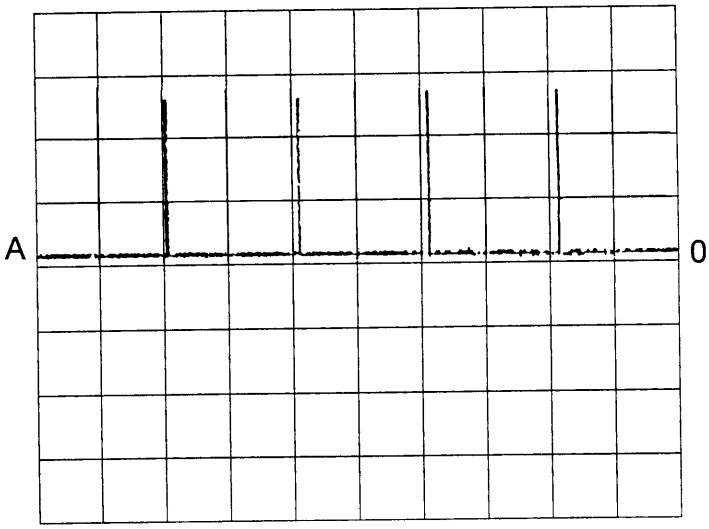
Signalchassis
CCU

PIN 1



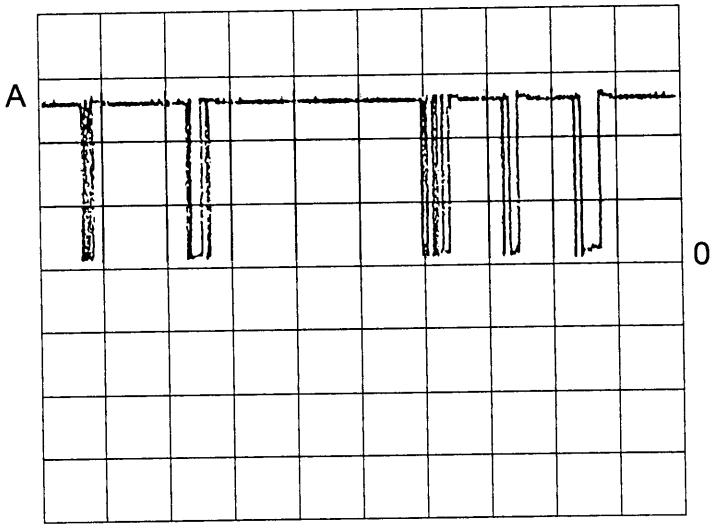
TIMEBASE .1 µsec/div
AMPL. 2 V/cm DC

PIN 3



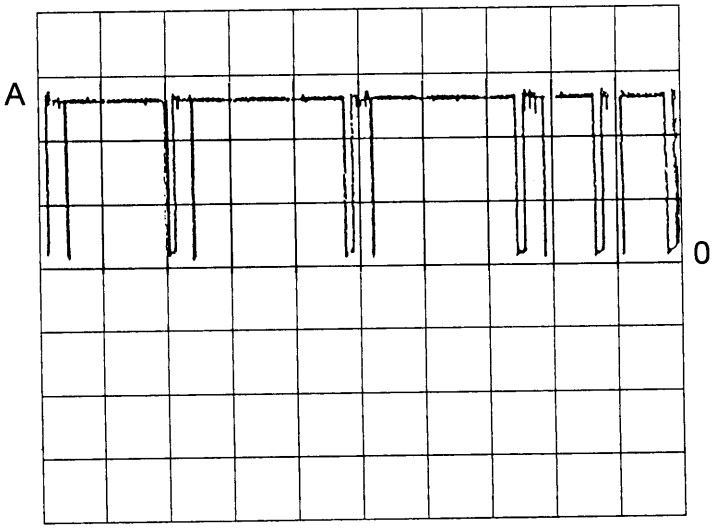
TIMEBASE .5 msec/div
AMPL. 2 V/cm DC

PIN 7 (Daten)



TIMEBASE .5 msec/div
AMPL. 2 V/cm DC

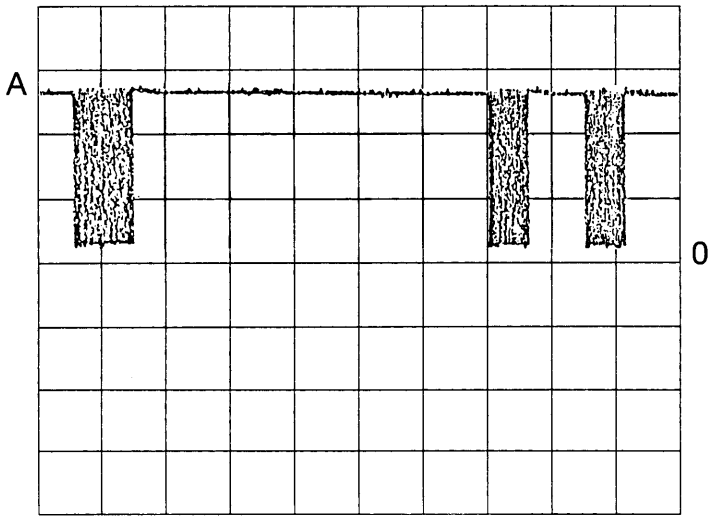
PIN 8 (Ident)



TIMEBASE .5 msec/div
AMPL. 2 V/cm DC

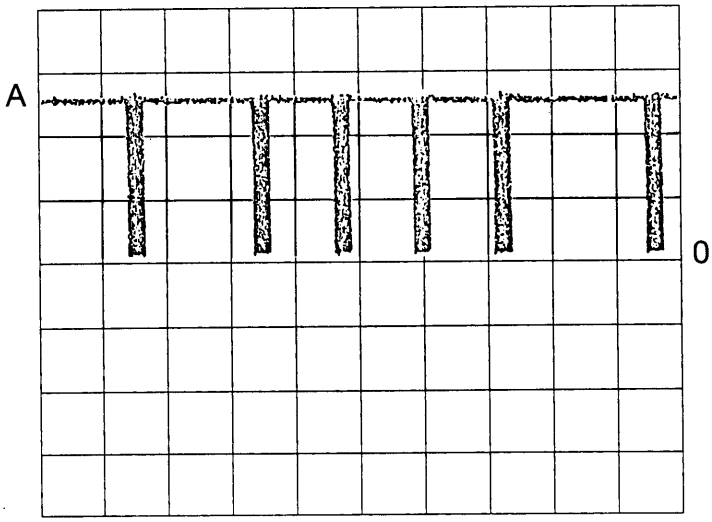
Signal-Chassis
CCU

PIN 9 (Clock)



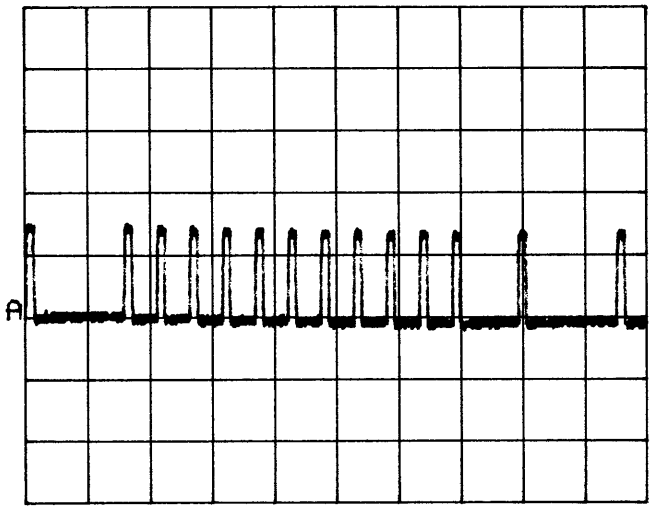
TIMEBASE .2 msec/div
AMPL. 2 V/cm DC

PIN 9 (Clock)



TIMEBASE .5 msec/div

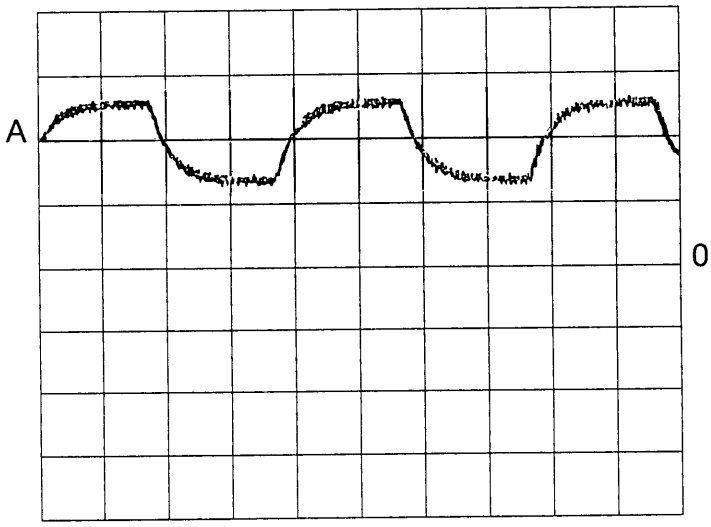
PIN 12 (IR-Signal)



TIMEBASE .2 msec/div
AMPL. 0.5 V/cm DC

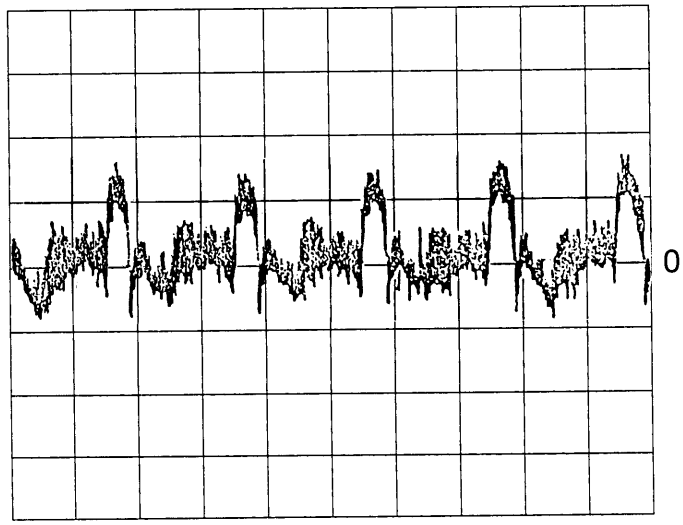
Signal-Chassis
CCU

CCU PIN 13
Channel 01



TIMEBASE .2 µsec/div
AMPL. 1 V/cm DC

PIN 14



TIMEBASE 10 msec/div
AMPL. 0,5 V/cm DC

VCU 2134
Video Codec

Video Codec

High-speed coder/decoder IC for analog-to-digital and digital-to-analog conversion of the video signal in digital TV receivers based on the DIGIT 2000 concept and having double-scan horizontal deflection. The VCU 2134 is a VLSI circuit in CI technology, housed in a 40-pin Dil plastic package. One single silicon chip combines the following functions and circuit details (see Fig. 1):

- two input video amplifiers
- one A/D converter for the composite video signal
- the noise inverter
- one D/A converter for the luminance signal
- two D/A converters for the color difference signals
- one RGB matrix for converting the color difference signals and the luminance signal into RGB signals
- three RGB output amplifiers
- programmable auxiliary circuits for blanking, brightness adjustment and picture tube alignment
- additional clamped RGB inputs for text and other analog RGB signals
- programmable beam current limiting

1. Functional Description

The VCU 2134 Video Codec Unit is intended for converting the analog composite video signal from the video demodulator into a digital signal. The latter is further processed digitally in the CVPU 2235 Video Processor, in the PSP 2210 Progressive Scan Processor, and in the DPU 2554 Deflection Processor. After processing in the CVPU and the PSP (color demodulation, comb filtering, line storage for double scanning etc.), the PSP's output signals (luminance and color difference) are reconverted into analog signals in the VCU 2134. From these analog signals are derived the RGB signals by means of the RGB matrix, and, after amplification in the internal RGB amplifiers, the RGB signals drive the RGB output amplifiers of the color TV receiver.

In addition, the VCU 2134 carries out the following functions:

- brightness adjustment
- automatic CRT spot-cutoff control (black level)
- white balance control and beam current limiting

Further, the VCU 2134 offers direct inputs for text or other analog RGB signals including adjustment of brightness and contrast for these signals.

The RGB matrix and RGB amplifier circuits integrated in the VCU 2134 are analog. The CRT spot-cutoff control is carried out via the RGB amplifiers' bias, and the white balance control is accomplished by varying the gain of these amplifiers. The VCU 2134 is clocked both by a 14 to 20.5 MHz clock signal and a 28 to 41 MHz clock signal supplied by the MCU 2632 Clock Generator IC.

1.1. The A/D Converter with Input Amplifiers and Bit Enlargement

The video signal is input to the VCU 2134 via pin 37 which is intended for normal TV video signal and for VCR or SCART video signal respectively. The video amplifier whose action is required, is activated by the CCU 2030, CCU 2050 or CCU 2070, via the IM bus by software (see Fig. 9). Video Amp I has the low gain (2 V video amplitude required), and Video Amp II has the high gain (1 V video amplitude required).

The amplification of both video amplifiers is doubled during the undelayed horizontal blanking pulse (at pin 36) in order to obtain a higher digital resolution of the color synchronization signal (burst).

The A/D converter is of the flash type, a circuit of 2^n comparators connected in parallel. This means that the number of comparators must be doubled if one additional bit is needed. Thus it is important to have as few bits as possible. For a slowly varying video signal, 8 bits are required. In order to achieve an 8-bit picture resolution using a 7-bit converter, a trick is used: during every other line the refer-

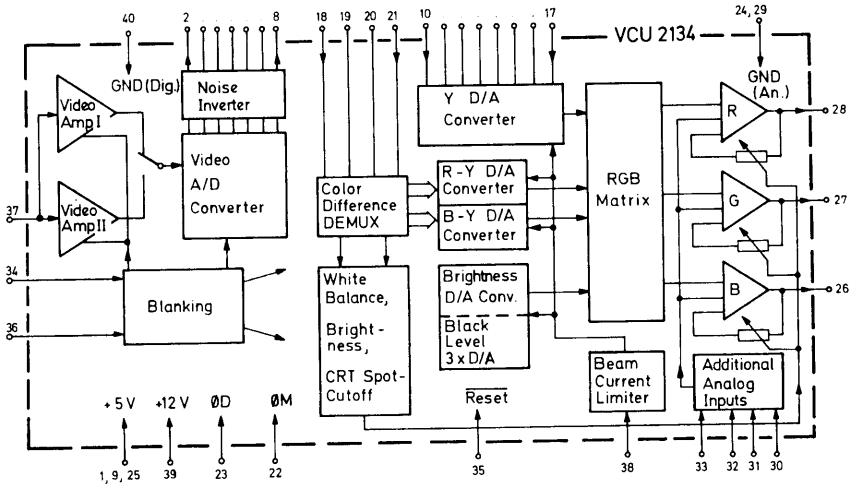


Fig. 1: Block diagram of the VCU 2134 Video Codec Unit

ence voltage of the A/D converter is changed by an amount corresponding to one half of the least significant bit. In this procedure, a grey value located between two 7-bit steps is converted to the next lower value during one line and to the next higher value during the next line. The two grey values on the screen are averaged by the viewer's eye, thus producing the impression of grey values with 8-bit resolution.

The A/D converter's sampling frequency is 14 to 20.5 MHz, the clock being supplied by the MCU 2632 Clock Generator IC which is common to all circuits for the digital TV system. The converter's resolution is 1/2 LSB of 8 bits. Its output signal is Gray-coded to eliminate spikes and glitches resulting from different comparator speeds or from the coder itself. The output is fed to the CVPU 2235 and to the DPU 2554 in parallel form.

1.2. The Noise Inverter

The digitized composite video signal passes the noise inverter circuit before it is put out to the CVPU and to the DPU 2554. The noise inverter serves for suppressing bright spots on the screen which can be generated by noise pulses, p. ex. produced by ignition sparks of cars etc. The function of the noise inverter can be seen in Fig. 2. The maximum white level corresponds with step 126 of the A/D converter's output signal (that means a voltage of 7 V at pin 37 in the case Video Amp I being selected). If, due to an unwanted pulse on the composite video signal, the voltage reaches 7.5 V (what means step 127 in digital) or more, the signal level is reduced by such an amount, that a medium grey is obtained on the screen (about 40 IRE). The noise inverter circuit can be switched off by software (address 16 in the CVPU, see there).

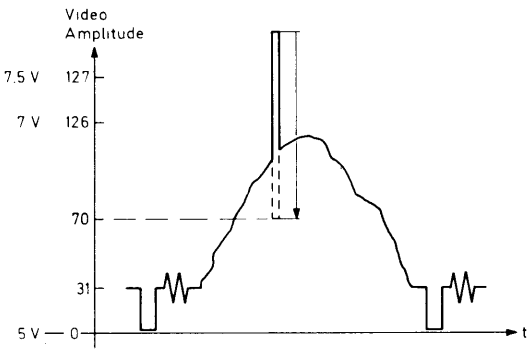


Fig. 2: Principle of the noise inverter

1.3. The Luminance D/A Converter (Y)

After having been processed in the CVPU 2235 (color demodulation, comb filtering, etc.) and in the PSP 2210, the different parts of the digitized video signal are fed back to the VCU 2134 for further processing to drive the RGB output amplifiers. The luminance signal (Y) is routed to the Y D/A converter in the VCU 2134 in the form of a parallel 8-bit signal with a resolution of 1/2 LSB of 9 bits. This bit range provides a sufficient signal range for contrast as well as positive and negative overshoot caused by the peaking filter (see Data Sheet CVPU).

The luminance D/A converter is designed as an R-2R ladder network. It is clocked with the 28.6 MHz clock signal applied to pin 23. The cutoff frequency of the luminance signal is determined by the clock frequency.

1.4. The D/A Converters for the Color Difference Signals R-Y and B-Y

In order to save input and output pins at the VCU 2134, CVPU and PSP as well as connection lines, the two digital color difference signals R-Y and B-Y are transferred in time multiplex operation. This is possible because these signals' bandwidth is only 2 MHz and the clock is a 28 to 41 MHz signal.

The two 8-bit D/A converters R-Y and B-Y are also built as R-2R ladder networks. They are clocked with ¼ clock frequency, but the clock for the multiplex data transfer is 28 to 41 MHz. Four times 4 bits are transferred sequentially, giving a total of 16 bits. A sync signal coordinates the multiplex operations in the VCU 2134, CVPU and PSP. Thus, only four lines are needed for 16 bits. Fig. 4 shows the timing diagram of the data transfer described.

To switch the C0 input the VCU 2134 from chroma signal reception to sync signal reception, the information to do this is given by the PSP to pins 10 to 17 of the VCU in the shape of "zero luminance" during horizontal blanking time. To avoid mistakes, a limiter in the PSP ensures that no zero luminance is put out at other times.

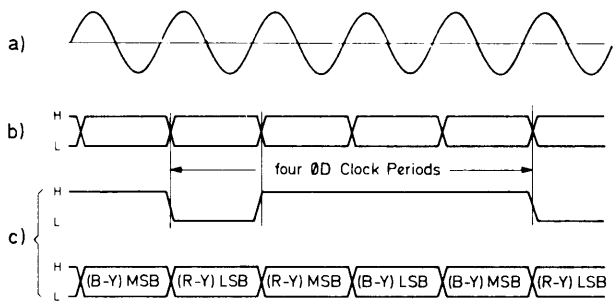


Fig. 4:
Timing diagram of the multiplex data transfer of the chroma channel between PSP and VCU 2134. The timing diagram between CVPU and PSP is identical except for the clock frequency which is only one half in that case.

a) double-scan clock ØD out of PSP

b) valid data out of the PSP

c) MUX data transfer of the chroma signals from PSP to VCU 2134. Upper line: sync pulse from pin 8/PSP to pin 21/VCU during sync time in horizontal blanking time, see Fig. 7b. Lower line: valid data from pins 8 to 11/PSP to pins 18 to 21/VCU

1.5. The RGB Matrix and the RGB Output Amplifiers

In the RGB matrix, the signals Y, R-Y and B-Y are dematrixed, the reduction coefficients of 0.88 and 0.49 being taken into account. In addition, the matrix is supplied with a signal produced by an 8-bit D/A converter for setting the brightness of the picture. The brightness adjustment range corresponds to ½ of the luminance signal range. It can be covered in 255 steps. The brightness is set by commands fed from the CCU 2030, CCU 2050 or CCU 2070 Central Control Unit to the CVPU via the IM bus.

There is available one matrix, called matrix 1, based on the formula:

$$R = r_1 \cdot (R\text{-}Y) + r_2 \cdot (B\text{-}Y) + Y$$

$$G = g_1 \cdot (R\text{-}Y) + g_2 \cdot (B\text{-}Y) + Y$$

$$B = b_1 \cdot (R\text{-}Y) + b_2 \cdot (B\text{-}Y) + Y$$

Table 1:
Values for the RGB matrix of the VCU 2134

Coefficient	Matrix 1
r_1	0.93
r_2	–0.12
g_1	–0.24
g_2	–0.17
b_1	0
b_2	1
VCU 2134:	Brand E

The three RGB output amplifiers are impedance converters having a low output impedance, an output voltage swing of 6 V (p-p), thereof 3 V for the video part and 3 V for brightness and dark signal. The output current is 4 mA. Fig. 5 shows the recommended video output stage configuration.

For the purpose of white-balance control, the amplification factor of each output amplifier can be varied stepwise in 127 steps (7 bits) by a factor of 1 to 2. Further, the CRT spot-cutoff control is accomplished via these amplifiers' bias by adding the output signal of an 8-bit D/A converter to the intelligence signal. The amplitude of the output signal corresponds to one half of the luminance range. The eight bits make it possible to adjust the dark voltage in 0.5 % steps. By means of this circuit, the factory-set values for the dark currents can be maintained and aging of the picture tube compensated.

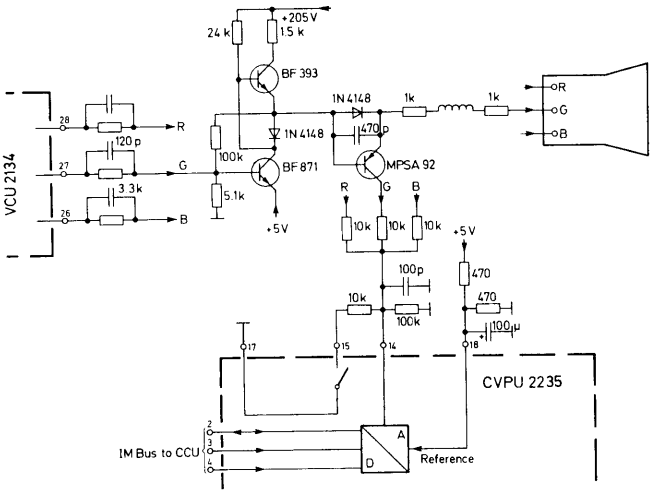


Fig. 5: Video output stage connected to the VCU 2134

1.6. The Beam Current and Peak Beam Current Limiter

The principle of this circuitry may be explained by means of Fig. 6. Both facilities are carried out via pin 38 of the VCU 2134. For beam current limiting and peak beam current limiting, contrast and brightness are reduced by reducing the reference voltages for the D/A converters Y, R-Y and B-Y. At a voltage of more than +4 V at pin 38, contrast and brightness are not affected. In the range of +4 V to +3 V, the contrast is continuously reduced. At +3 V, the original contrast is reduced to a programmable level, which is set by the bits of address 16 of the CVPU as shown in Table 2. A further decrease of the voltage merely reduces brightness, the contrast remains unchanged. At 2.5 V, the brightness is reduced to zero. At voltages lower than 2 V, the output goes to ultra black. This is provided for security purposes.

The beam current limiting is sensed at the ground end of the EHT circuit, where the average value of the beam current produces a certain voltage drop across a resistor inserted between EHT circuit and ground. The peak beam current limiting can be provided additionally to avoid "blooming" of white spots or letters on the screen. For this, a fast peak current limitation is needed which is sensed by three sensing transistors inserted between the RGB amplifiers and the cathodes of the picture tube. One of these three transistors is shown in Fig. 6. The sum of the picture tube's three cathode currents produces a voltage drop across resistor R1. If this voltage exceeds that generated by the divider R2, R3 plus the base emitter voltage of T2, this transistor will be turned on and the voltage at pin 38 of the VCU 2134 sharply reduced. Time constants for both beam current limiting and peak beam current limiting can be set by the capacitors C1 and C2.

Table 2: Code of the contrast reduction bits (Addr. 16)

I	m	Contrast Reduction	
		%	dB
0	0	10	−20
0	1	30	−10
1	0	50	− 6
1	1	70	− 3

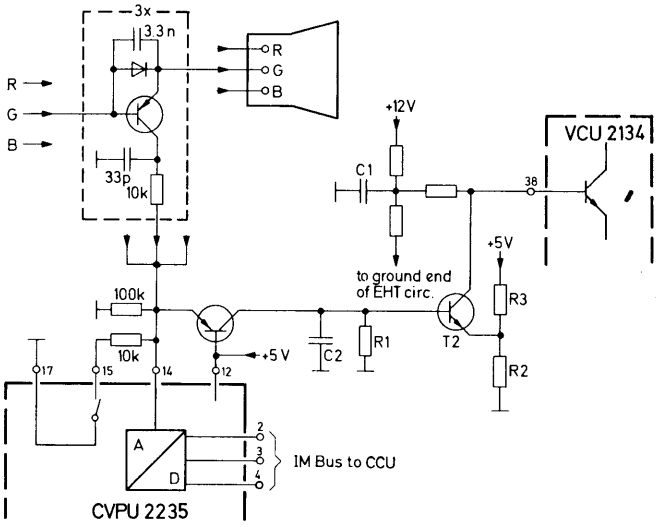


Fig. 6: Beam current and peak beam current limiter

1.7. The Blanking Circuit

The blanking circuit coordinates blanking during vertical and horizontal flyback. During the latter, the VCU 2134's output amplifiers are switched to "ultra black". Such switching is different during vertical flyback, however, because at this time the measurements for picture tube alignment are carried out. During vertical flyback, only the cathode to be measured is switched to "black" during measuring time, the other two are at ultra black so that only the dark current of one cathode is measured at the same time. For measuring the leakage current, all three cathodes are switched to ultra black.

The sequence described is controlled by three code bits contained in a train of 72 bits which is transferred from the CVPU through PSP to the VCU 2134 during each vertical blanking interval. This transfer starts with the vertical blanking pulse. During the transfer all three cathodes of the picture tube are biased to ultra black. In the same manner, the white-balance control is done.

The blanking circuit is controlled by two pulse combinations supplied by the DPU 2554 Deflection Processor ("sandcastle pulses"). Pin 34 of the VCU 2134 receives the combined vertical blanking and delayed horizontal blanking pulse from pin 22 of the DPU (Fig. 7b), and pin 36 of the VCU gets the combined undelayed horizontal blanking and color key pulse from pin 19 of the DPU (Fig. 7a). The two outputs of the DPU are tristate-controlled, supplying the output levels max. 0.4 V (low), min. 4.0 V (high), or high-impedance, whereby the signal level in the high-impedance mode is determined by the VCU's input configuration, a voltage divider of 3.6 kΩ and 4.7 kΩ between the +5 V supply and ground, to 2.8 V. The VCU's input amplifier has two thresholds of 2.0 V and 3.4 V for detecting the three levels of the combined pulses. In this way, two times two pulses are transferred via only two lines.

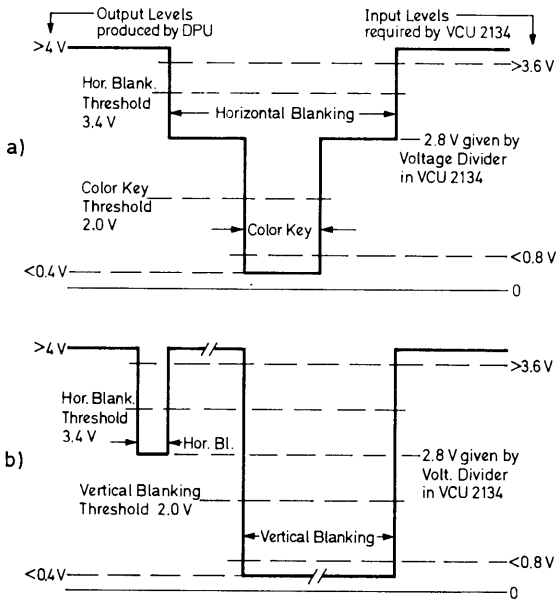


Fig. 7: Pulses which control the VCU's blanking circuit
a) combined undelayed horizontal blanking and color key pulse (pin 36)
b) combined delayed horizontal blanking and vertical blanking pulse (pin 34)

1.8. The Circuitry for Picture Tube Alignment

During vertical flyback, a number of measurements are taken and data is exchanged between the VCU 2134, the CVPU via PSP and the CCU. This measurements deal with picture tube alignment, as white level and dark current adjustment, and with the photo current supplied by a photo resistor which serves for adapting the contrast of the picture to the light in the room where the TV set is operated (the latter feature only in connection with the CVPU 2235, see Fig. 5). The circuitry for transferring the picture tube alignment data, the sensed beam currents and the photo current is clocked in compliance with the PSP 2210 by the vertical blanking pulse and the color key pulse. To carry out the measurements, a quadruple cycle is provided (see Table 3). The timing of the data transfer during the vertical flyback is shown in Fig. 8, and Fig. 9 shows the data sequence during that data transfer.

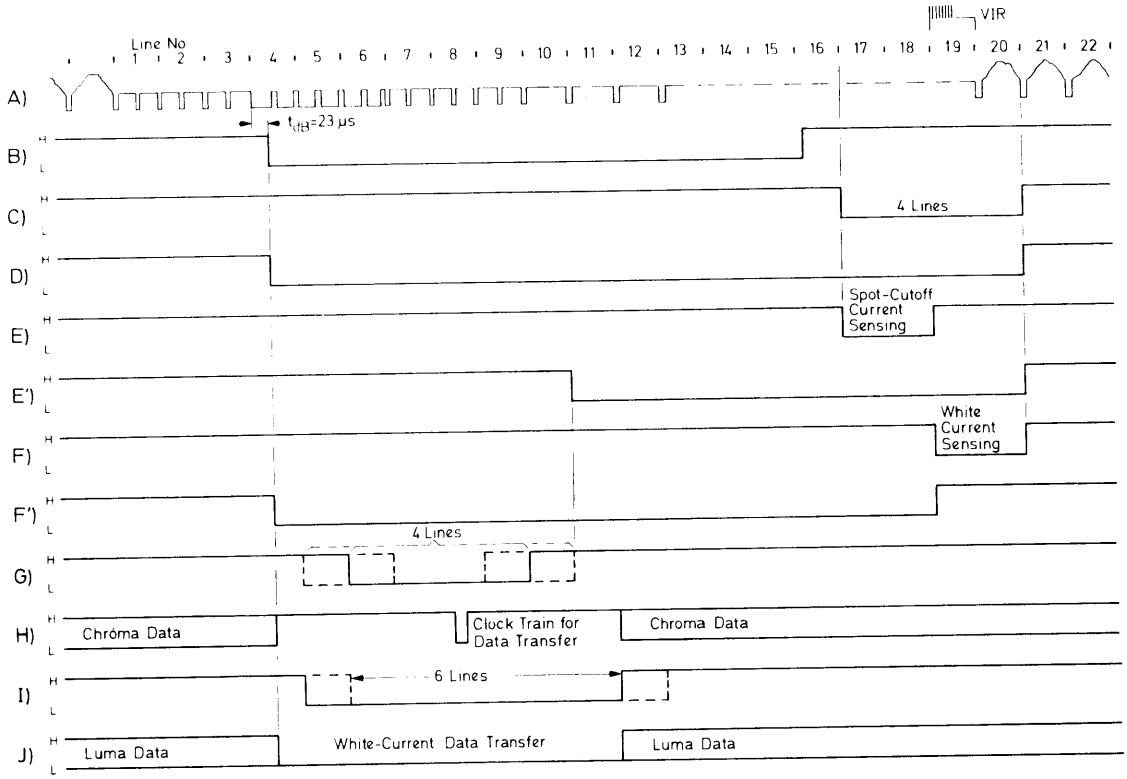


Fig. 8: Data transfer during vertical flyback

A) Video signal during vertical flyback, lines No. 1 to 22.

B) Vertical blanking pulse supplied by pin 22 of the DPU 2554 to pin 34 of the VCU 2134 (t_{aB}), duration is 13 lines and delay with respect to the start of line 4 is t_{dB} = 23 µs. With this pulse starts the 72-bit data transfer described in section 1.7., and with the end of pulse starts the picture tube's cathode current measurement.

C) Internal control pulse for CRT current measurement, generated simultaneously in VCU 2134 and CVPU. The cathode under test is set to black by code bits.

D) Internal control pulse generated in VCU 2134 (pulse B + pulse C). During this pulse the cathodes of the CRT are at ultra black, the D/A converters for chroma and brightness are set to zero output, and Teletext fast blanking is off.

E) Control pulse generated in CVPU and VCU 2134 for CRT spot-cutoff current sensing. During this time, the measured output is set to black level.

E') Control pulse generated in VCU 2134. During this pulse, the output of the Y D/A converter delivers the white-current measuring level. This is achieved by switching off the clock for the D/A converter.

F) Control pulse generated in VPU and VCU for white current sensing. During this time, the measured output is set to white current measuring level.

F') Control pulse generated in VCU 2134 which sets the Y D/A converter to zero output by setting its reference voltage to zero.

G) Window pulse for 72-bit data transfer from CVPU to VCU as described in section 1.7., duration 4 lines, generated in VCU 2134. The end of this pulse starts the clock hold-off time for the Y D/A converter (diagram E').

H) Signal at the C0/Msync output of the PSP supplied to the C0/Msync input of the VCU 2134 (pin 21). Normally, via this connection are transferred chroma data and the sync signal. With the begin of the vertical blanking, chroma data transfer is interrupted to enable the transfer of 72 clock pulses for 72-bit data transfer.

I) Window pulse for 72-bit data transfer, generated in CVPU, duration 6 lines. The end of this pulse enables Y and chroma data output from CVPU to VCU.

J) Signals at the L0 to L7 outputs of the PSP supplied to the L0 to L7 inputs (pins 10 to 17) of the VCU 2134. With the begin of vertical blanking, luma data transfer is interrupted and the luminance output of the CVPU supplies white-current measuring level during lines 19 and 20 (see diagram F).

Table 3: Test cycles during four consecutive vertical blanking periods

Half Picture No.	Test carried out	Code Bit PSP→ VCU R	G	B	Code Bit PSP→ CCU	
1	Cathode leakage currents and photo current	1	1	1	0	0
2	Dark current Red, and white level Red	0	1	1	0	1
3	Dark current Green, and white level Green	1	0	1	1	0
4	Dark current Blue, and white level Blue	1	1	0	1	1

Code bit 1 means that the corresponding output amplifier of the VCU 2134 delivers the signal "ultra black" to the output amplifier connected to it.

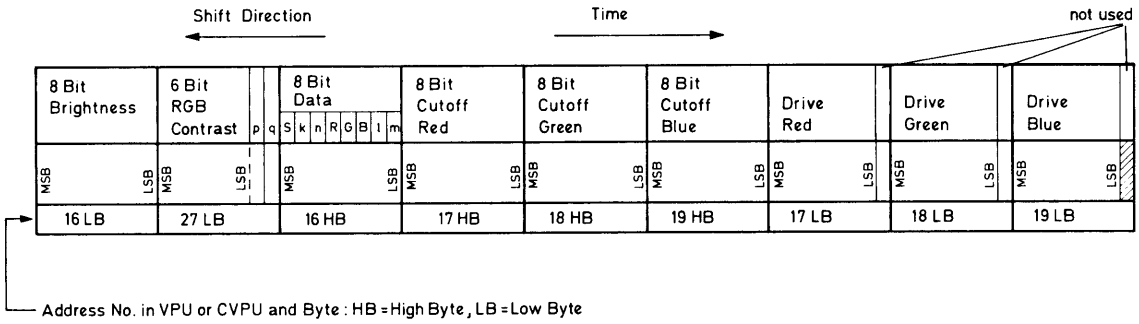


Fig. 9:
Data sequence during the transfer of test results from the CVPU to the VCU 2134. Nine Bytes are transferred, in each case the MSB first. These 9 Bytes, 8 bits each, coincide with the 72 pulses of 4.4 MHz that are transferred during vertical flyback from pin 8 of the PSP to pin 21 of the VCU 2134 (see Fig. 8).
l and m: beam current limiter range
k: noise inverter on/off
n: video input amplifier switching bit
n = 0 means Video Amp I selected (input amplitude 2 V)
n = 1 means Video Amp II selected (input amplitude 1 V)
S: clamping mode:
S = 0 means clamping by color key pulse at pin 36
S = 1 means clamping by additional pulse (Fig. 10)
R, G, B: code bits
p = 1: no doubled gain in the input amplifier during horizontal blanking (see section 1.1.)
q = 1: no changing of the A/D converter's reference voltage during every other line (see section 1.1.)

1.9. The Analog RGB Inputs

The three additional analog RGB inputs are provided for inputting text or other analog RGB signals. They are connected to fast voltage-to-current converters whose output current can be altered in 64 steps (6 bits) for contrast setting between 100 % and 30 %. The three inputs are clamped to a DC black level which corresponds to the level of 31 steps in the luminance channel, by means of either the color key pulse or an additional pulse provided by a modified fast switching input. The mode is selected by the shift register (Fig. 9). So, the same brightness level is achieved for normal and for external RGB signals. The output currents of the converters are then fed to the three RGB output amplifiers. Switchover to the external video signal is also fast.

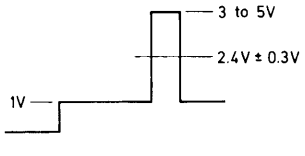


Fig. 10: Shape of the fast switching and clamping pulses at pin 33

2. Outline Dimensions and Pin Connections

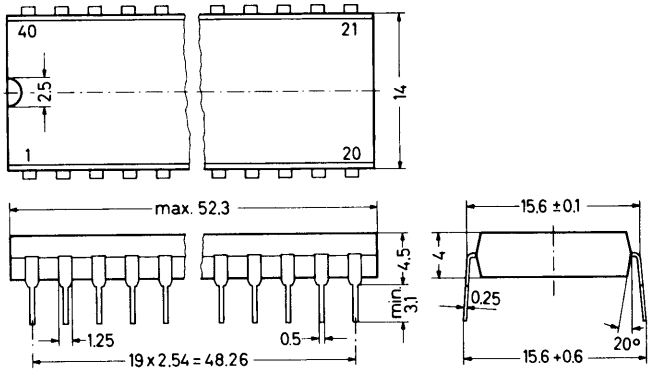


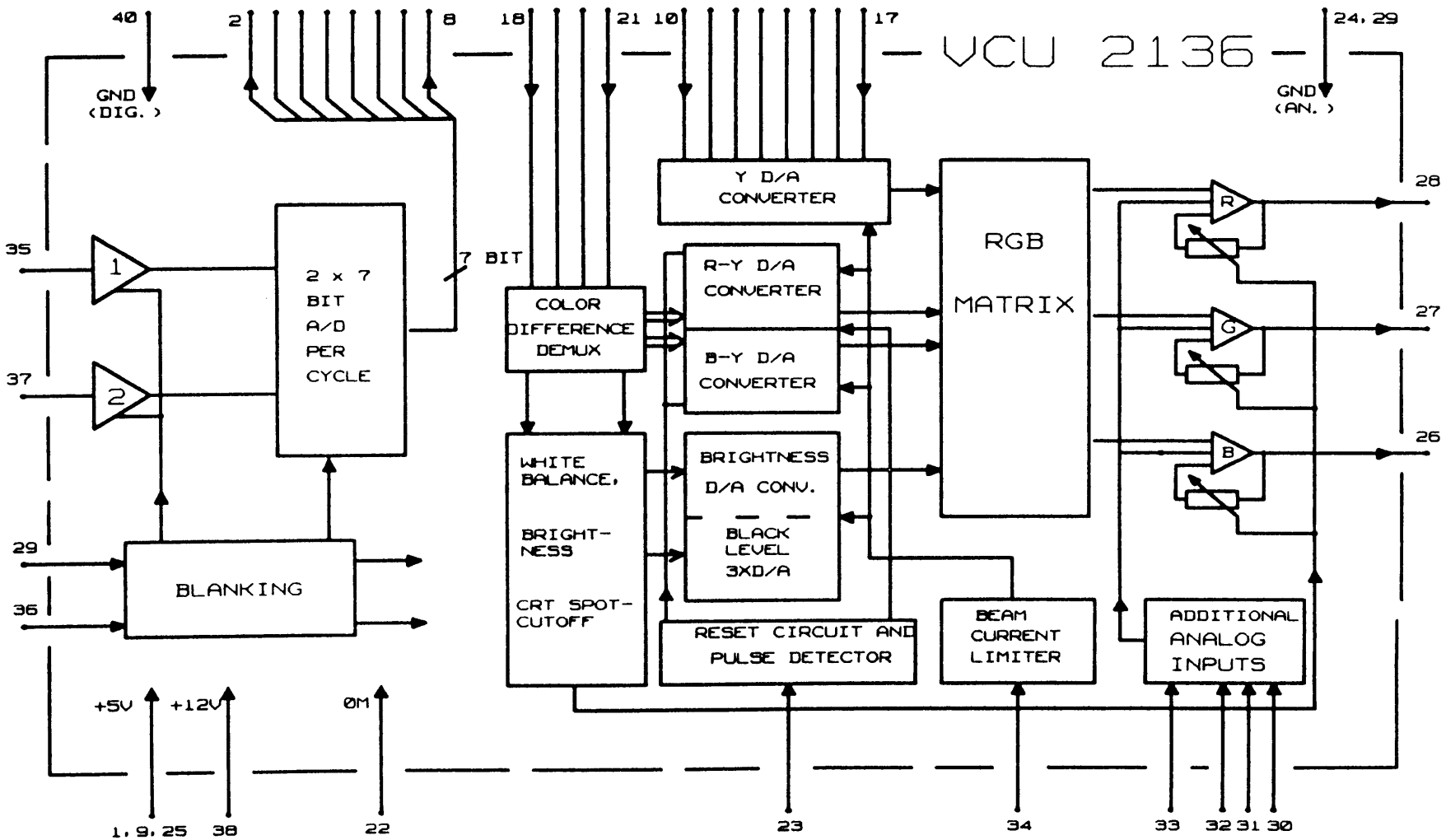
Fig. 11:
VCU 2134 in 40-pin Dil Plastic Package,
20 B 40 according to DIN 41 870

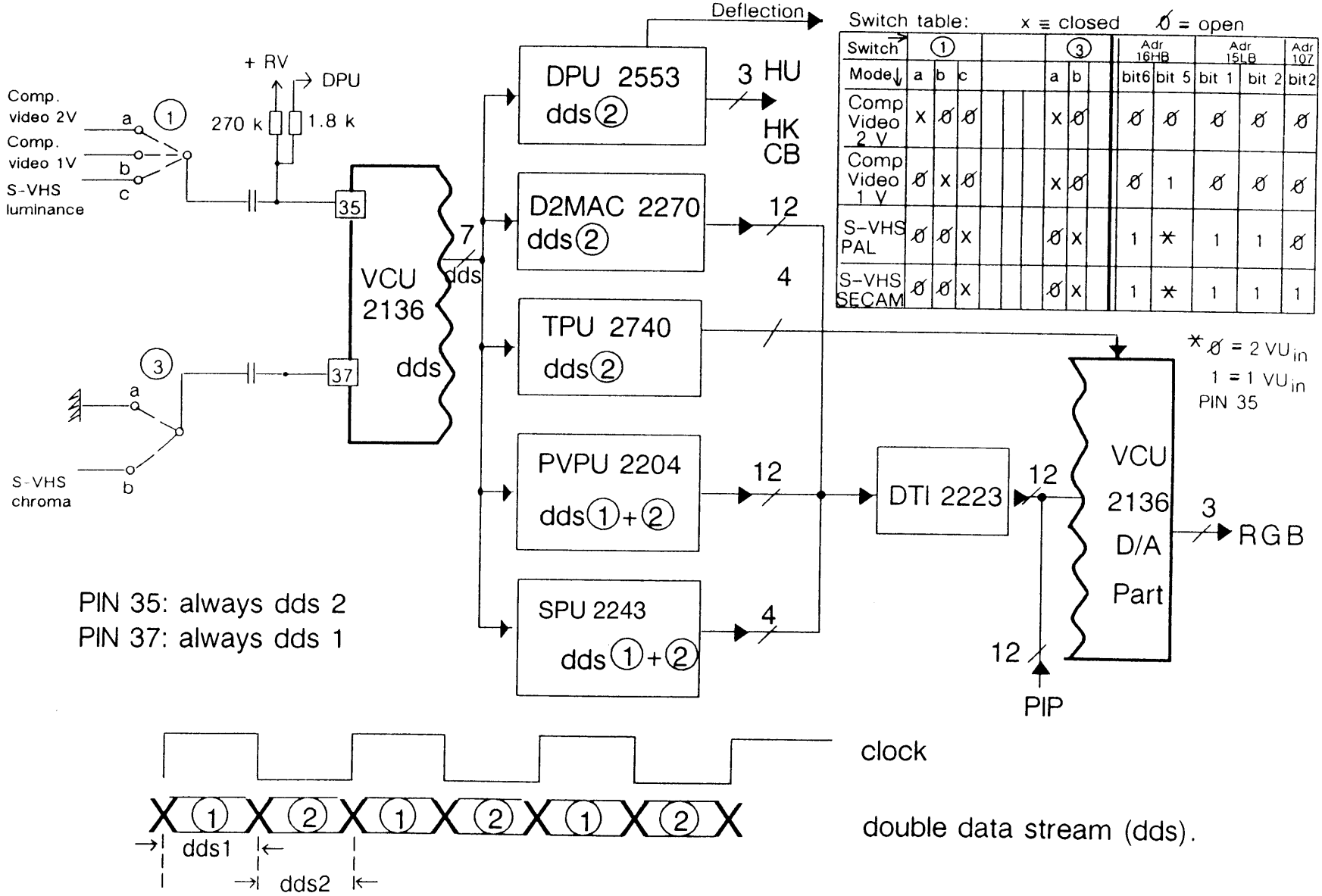
Weight approx. 6 g Dimensions in mm

Pin Connections

1	Supply Voltage, +5 V
2	V0 Digital Video Output (LSB)
3	V1 Digital Video Output
4	V2 Digital Video Output
5	V3 Digital Video Output
6	V4 Digital Video Output
7	V5 Digital Video Output
8	V6 Digital Video Output (MSB)
9	Digital Supply Voltage, +5 V
10	L7 Luma Input (MSB)
11	L6 Luma Input
12	L5 Luma Input
13	L4 Luma Input
14	L3 Luma Input
15	L2 Luma Input
16	L1 Luma Input
17	L0 Luma Input (LSB)
18	C1 Chroma Input
19	C2 Chroma Input
20	C3 Chroma Input (MSB)
21	C0 Chroma and Msync Input (LSB)
22	ØM Main Clock Input
23	ØD Double-Scan Clock Input
24	Analog Ground, 0
25	Supply Voltage, +5 V
26	B Output
27	G Output
28	R Output
29	Analog Ground, 0
30	Analog B Input
31	Analog G Input
32	Analog R Input
33	Fast Switching Input
34	Vertical Blanking and Delayed Horizontal Blanking Input
35	$\overline{\text{Reset}}$ Input
36	Undelayed Hor. Blanking and Color Key Pulse Input
37	Analog Video Signal Input
38	Beam Current Limiter Input
39	Supply Voltage, +12 V
40	Digital Ground, 0

VCU 2136


VCU 2136
40
GND (DIG.)
2
8
18
21 10
17
24, 29
GND (AN.)
35
37
1
2
2 x 7 BIT A/D PER CYCLE
7 BIT
COLOR DIFFERENCE DEMUX
Y D/A CONVERTER
R-Y D/A CONVERTER
B-Y D/A CONVERTER
RGB MATRIX
R
G
B
28
27
26
29
36
BLANKING
WHITE BALANCE,
BRIGHT-NESS
CRT SPOT-CUTOFF
BRIGHTNESS D/A CONV.
BLACK LEVEL 3XD/A
RESET CIRCUIT AND PULSE DETECTOR
BEAM CURRENT LIMITER
ADDITIONAL ANALOG INPUTS
+5V
+12V
0M
1, 9, 25
38
22
23
34
33
32
31
30


Deflection
Switch table: x ≡ closed Ø = open
Switch ① ③ Adr 16HB Adr 15LB Adr 107
Mode ↓ a b c a b bit6 bit 5 bit 1 bit 2 bit2
Comp Video 2 V x Ø Ø x Ø Ø Ø Ø Ø Ø
Comp Video 1 V Ø x Ø x Ø Ø 1 Ø Ø Ø Ø
S-VHS PAL Ø Ø x Ø x 1 * 1 1 Ø
S-VHS SECAM Ø Ø x Ø x 1 * 1 1 1
* Ø = 2 VU in
1 = 1 VU in
PIN 35
+ RV
DPU
Comp. video 2V
Comp. video 1V
S-VHS luminance
S-VHS chroma
270 k
1.8 k
VCU 2136 dds
DPU 2553 dds②
3 HU
HK
CB
D2MAC 2270 dds②
TPU 2740 dds②
PVPU 2204 dds①+②
SPU 2243 dds①+②
DTI 2223
VCU 2136 D/A Part
RGB
PIP
PIN 35: always dds 2
PIN 37: always dds 1
clock
double data stream (dds).
dds1
dds2

VCU 2136 & VPU 2204

The VCU 2136 and VPU 2204 represent further developments of the VCU 2133 and VPU 2203 that are suitable for S-VHS. This application note describes the modifications that were necessitated for these ICs by the S-VHS. It should be read as an addendum to data sheets VCU 2133/5E and VPU 2203/1E.

Some improvements have been made in the luminance filters to get better frequency response and therefore better picture quality. See the part "New filters" in VPU 2204.

With S-VHS the luma and chroma information is transmitted in parallel channels. The luma and chroma data are converted by the VCU 2136 A/D converter and are transmitted in the time multiplex via the digital bus. It is important that a corresponding demultiplex takes place in the PVPU and that the SPU 2223 is able to separate the chroma information from the multiplexed data. Furthermore, the DTI 2223 is able to compensate group delay difference between the luma and chroma data.

Fig. 1 illustrates the timing of the data: the analog signals at the inputs V1 at pin 35 and V2 at pin 37 of the VCU 2136 are taken over in time multiplex and an A/D conversion is performed. As the timing diagram (fig. 1) shows, the data 1 (luma in S-VHS operation) are taken over with the rising edge and the data 2 with the falling edge of the clock signal. The data rate is doubled in comparison to the VCU 2133 (Double Data Stream DDS).

Changes from the VCU 2133 to the VCU 2136:

With the help of two control bits, three possible VCU operation modes "Composite Video", "VHS" and "S-VHS" can be set. First, these two bits are entered into register 16 of the VPU 2204 by the CCU. During the vertical blanking interval this information is passed on from the VPU to the VCU inside the 72 bit data stream. Composite Video, VHS and S-VHS operation modi of the VCU only differ in the setting of the input operation multipliers 1 and 2 (see fig. 2). The function of the input multiplexer remains unchanged.

The following constellations are possible. Refer to the VPU 2203/1E data sheet, table 3: "Data transfer between ...".

Address no. 16, high byte, bit 6=1,
Address no. 16, high byte, bit 5=0

"S-VHS mode"
Pin 35: Analog Luma, 2.0V max.
1 V input is also possible if high byte bit 5 = 1 in address 16
Pin 37: Analog Chroma, 0.3V max. for burst.

Address no. 16, high byte, bit 6=0,
Address no. 16, high byte, bit 5=0:

"Composite Video" mode
Amplification during color burst key x 2
Pin 35: Analog Composite Video, 2.0V max.
Pin 37: Analog Composite Video, 2.0V max.
only the data on pin 35 is processed in this mode.

Address no. 16, high byte, bit 6=0
Address no. 16, high byte, bit 5=1:

"VHS" mode.
Amplification during color burst key x 2
Pin 35: Analog Composite Video, 1.0V max.
Pin 37: Analog Composite Video, 1.0V max.
Only the data on pin 37 is processed in this mode.

Note: The VCU 2136 does not contain the noise inverter that was incorporated in the VCU 2133 any longer. Address no. 16, high byte bit 6 is the former bit "noise inverter".

Changes from the VPU 2203 to the VPU 2204:

- on the input side, a demultiplexer was inserted to separate the luma and chroma data in the double data stream and to distribute them into the luma and chroma channels of the VPU (see fig. 3).

- the colour trap was conceived to be switched off for the S-VHS operation mode.

- Two additional control bits were introduced (refer to the VPU 2203/1E data sheet table 3: "Data transfer between ..."), that is:

Address no. 15, low byte, bit 2 "S-VHS on" (see fig. 2):

bit 2=0: S-VHS off
VPU works on the V1 data only. Luma and chroma data are separated with the help of chroma trap and chroma filter.

bit 2=1: S-VHS on
demultiplex of the sequential luma and chroma data, no chroma x 2 during color burst.

Address no. 15., low byte, bit 1 (see fig. 3):

bit 1=0: chroma trap on.
bit 1=1: chroma trap off.

New filters in the VPU 2204

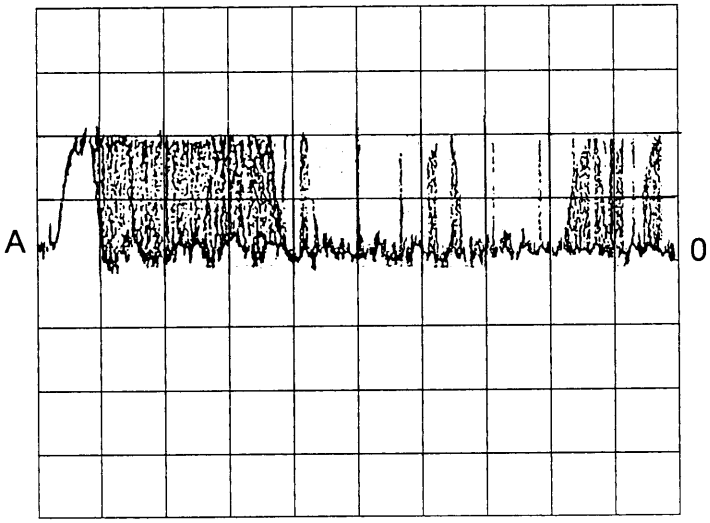
To improve frequency response and picture quality some changes in the luminance- and peaking filter part of the VPU have been made. The old filter characteristics are still available. New features are:

the S-VHS characteristics without chroma trap
the "enhanced" Munakami filter without ringing
the "broad" version.

For SECAM the broader chroma trap can be switched off to the same chroma trap as for PAL.

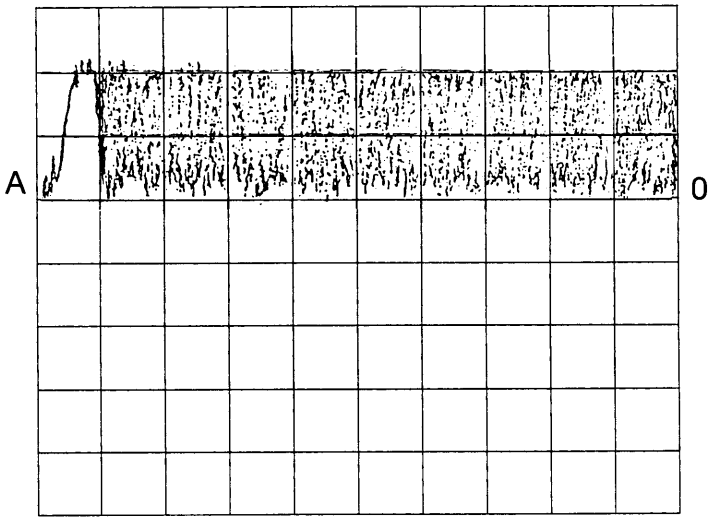
VCU 2136

PIN 10



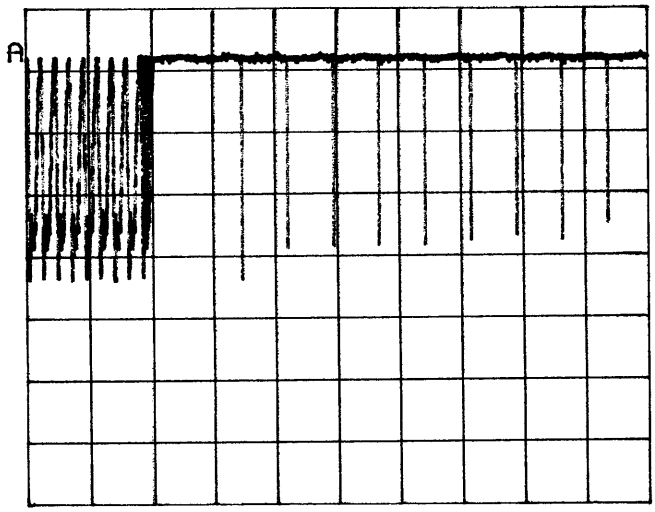
TIMEBASE .1 µsec/div
AMPL. 500mV/cm DC

PIN 11–17



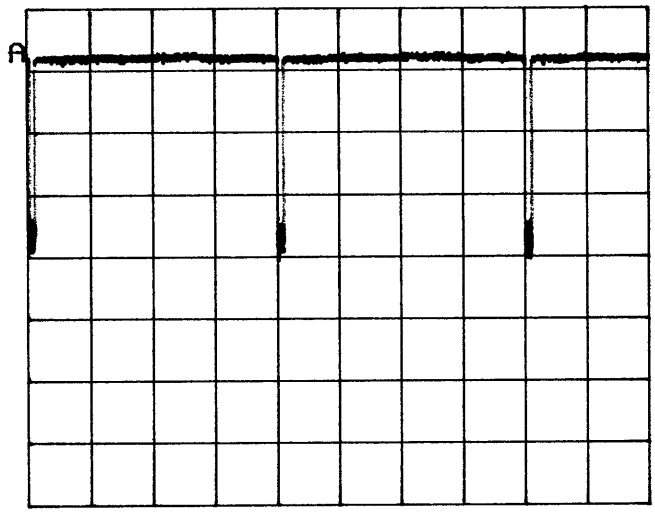
TIMEBASE .1 µsec/div
AMPL. 500mV/cm DC

PIN 18



TIMEBASE .5 µsec/div
AMPL. 0.5 V/cm DC

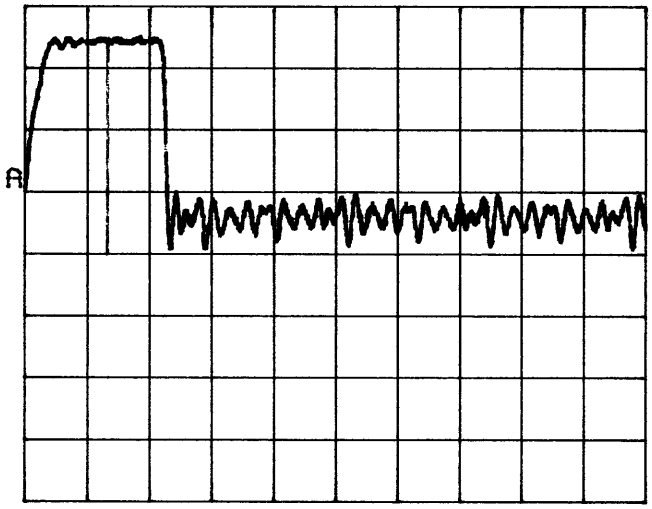
PIN 19



TIMEBASE 5 msec/div
AMPL. 0.5 V/cm DC

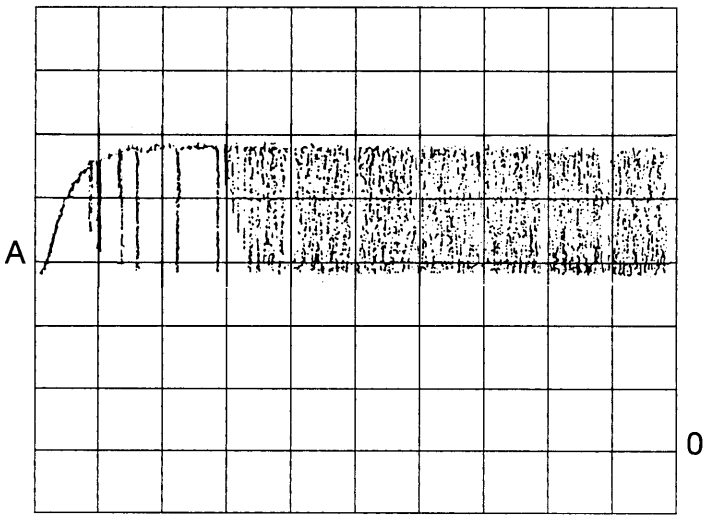
VCU

PIN 20



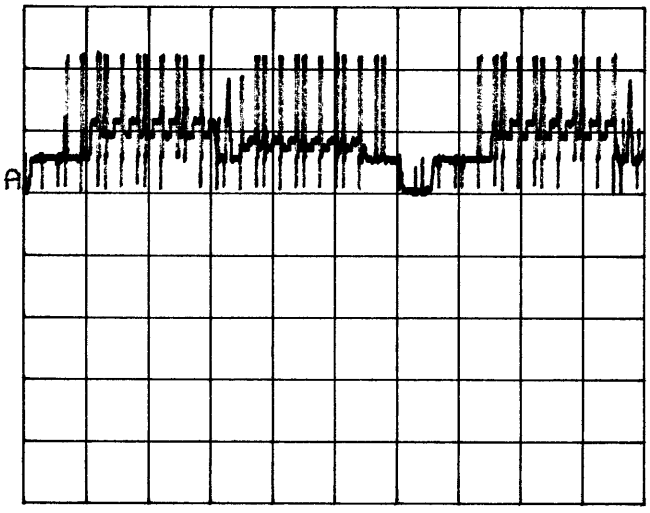
TIMEBASE .1 µsec/div
AMPL. 0,5 V/cm DC

PIN 23



TIMEBASE .1 µsec/div
AMPL. 2 V/cm DC

PIN 35



TIMEBASE 10 µsec/div
AMPL. 1 V/cm DC

DPU 2553, DPU 2554, DPU 2555 Deflection Processors

Deflection Processors

1. Introduction

These programmable VLSI circuits in N-channel MOS technology carry out the deflection functions in digital color TV receivers based on the DIGIT 2000 system and are also suitable for text and D2-MAC application. The three types are basically identical, but are modified according to the intended application:

DPU 2553 – normal-scan horizontal deflection, standard CTV receivers, also equipped with Teletext and D2-MAC facility

DPU 2554 – double-scan horizontal deflection, for CTV receivers equipped with double-frequency horizontal deflection and double-frequency vertical deflection for improved picture quality. At power-up, this version starts with double horizontal frequency.

DPU 2555 – normal scan horizontal deflection as DPU 2553, but with an extra flag for the IM bus, so that one DPU 2553 and one DPU 2555 may be operated simultaneously in one CTV receiver as is required for Teletext or Viewdata operation if increased deflection frequency is intended for high-quality text display. In this case, the DPU 2553 acts as sync separator for the received Teletext or Viewdata signal, whereas the DPU 2555 is used as deflection processor for the displayed page, or vice versa.

1.1. General Description

The DPU 2553/54/55 Deflection Processors contain the following circuit functions on one single silicon chip:

- video clamping
- horizontal and vertical sync separation
- horizontal synchronization
- normal horizontal deflection
- east-west correction, also for flat-screen picture tubes
- vertical synchronization
- normal vertical deflection
- sawtooth generation
- text display mode with increased deflection frequencies (18.7 kHz horizontal and 60 Hz vertical)
- D2-MAC operation mode

and for DPU 2554 only:

- double-scan horizontal deflection
- normal and double-scan vertical deflection

In this data sheet, all information given for double-scan mode is available with the DPU 2554 only. Types DPU 2553 and DPU 2555 start the horizontal deflection with 15.5 kHz according to the normal TV standard, whereas type DPU 2554 starts with 31 kHz according to the double-scan system. The only difference between types DPU 2553 and DPU 2555 is in the function of the flag IMS which enables and disables the IM bus interface of the respective deflection processor. With this, it is possible to operate both types in parallel on the same IM bus, as is required for the Teletext or Viewdata display mode with increased deflection frequencies.

The following characteristics are programmable:

- selection of the TV standard (PAL, D2-MAC or NTSC)
- selection of the deflection standard (Teletext, horizontal and vertical double-scan, and normal scan)
- filter time-constant for horizontal synchronization
- vertical amplitude, S correction, and vertical position for in-line, flat-screen and Trinitron picture tubes
- east-west parabola, horizontal width, and trapezoidal correction for in-line, flat-screen and Trinitron picture tubes
- switchover characteristics between the different synchronization modes
- characteristic of the synchronism detector for PLL switching and muting

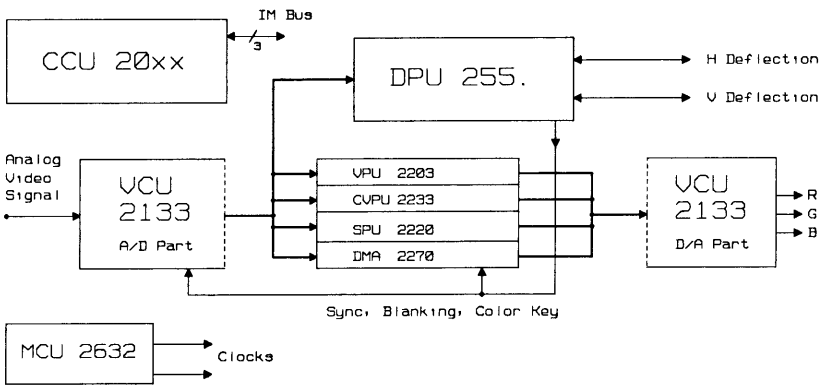


Fig. 1-1: Block diagram of the video and deflection section of a digital TV receiver according to the DIGIT 2000 concept

1.2. Environment

Fig. 1-1 shows the simplified block diagram of the video and deflection section of a digital TV receiver based on the DIGIT 2000 system. The analog video signal derived from the video detector is digitized in the VCU 2133 Video Codec and supplied in a parallel 7 bit Gray code. This digital video signal is fed to the video section (VPU, CVPU, SPU and DMA) and to the DPU 2553/54/55 Deflection Processor which carries out all functions required in conjunction with deflection, from sync seperation to the control of the deflection power stages, as described in this data sheet.

2. Specifications

2.1. Outline Dimensions

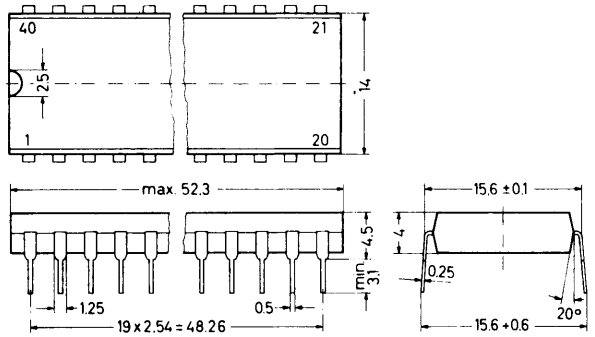


Fig. 2-1:
DPU 2553, DPU 2554 and DPU 2555 in 40-pin Dil plastic package, 20 B 40 according to DIN 41 870

Weight approx. 6 g Dimensions in mm

2.2. Pin Connections

1 Ground
2 ∅M Main Clock Input
3 Output for Single-Scan Vertical Blanking Pulse
4 Clamping Output 2
5 $\overline{\text{Reset}}$ Input
6 Input for the D2-MAC Composite Sync Signal and Output for the Separated Composite Sync Signal
7 1H and 2H Skew Data Output
8 V_{SUP} Supply Voltage
9 V6 Video Input (MSB)
10 V5 Video Input
11 V4 Video Input
12 V3 Video Input
13 V2 Video Input
14 V1 Video Input
15 V0 Video Input (LSB)
16 IM Bus Clock Input
17 IM Bus Ident Input
18 IM Bus Data Input/Output
19 Combined Output for the Color Key Pulse and the Undelayed Horizontal Blanking Pulse
20 Ground
21 Clamping Output 1
22 Combined Output for the Delayed Horizontal Blanking Pulse and the Vertical Blanking Pulse
23 Horizontal Flyback Input
24 Undelayed Horizontal Blanking Output
25 Vertical Flyback Safety Input
26 Vertical Flyback Output
27 Vertical Sawtooth Output
28 East-West Parabola Output
29 Horizontal Output Polarity Select Input and Start Oscillator Pulsewidth Select Input
30 Ground
31 Horizontal Output
32 V_{SUP} Supply Voltage
33 External Standard Selection Input
34 Start Oscillator Clock Input
35 Start Oscillator Supply Voltage
36 Start Oscillator Select Input
37 Control Switch Output for the Horizontal Power Stage
38 Test Pin, leave vacant
39 Interlace Control Output
40 V_{SUP} Supply Voltage

2.3. Pin Descriptions

Pins 1, 20 and 30 – Ground
These pins must be connected to the negative of the supply.

Pins 2 – ∅M Main Clock Input (Fig. 2-4)
By means of this input, the DPU receives the required main clock signal from the MCU 2600 or MCU 2632 Clock Generator IC.

Pin 3 – Single-Scan Vertical Blanking Output (Fig. 2-11)
In vertical double-scan mode, this pulse is also required by the CVPU 2235 Comb Filter Video Processor.

Pins 4 and 21 – Clamping Outputs 2 and 1 (Fig. 2-10)
These pins supply pulses for clamping the video signal at the VCU 2133 or VCU 2134 during the back porch.

Pin 5 – $\overline{\text{Reset}}$ Input (Fig. 2-2)
This pin is used for hardware reset. At low level, reset is actuated, and at high level the DPU is ready for communication with the CCU via the IM bus.

Pin 6 – Input for the D2-MAC Composite Sync Signal and Output for the Separated Composite Sync Signal
This pin (Fig. 2-9) is the input for the D2-MAC composite sync signal and the output for the separated composite sync signal.

Pin 7 – Skew Data Output (Fig. 2-10)
This pin delivers the 1H and 2H skew data stream required by the PSP 2210 or PSP 2032 Progressive Scan Processor and the TPU 2732 or TPU 2733 or TPU 2740 Teletext Processor or others for adjusting the phase of the double-scan video signal and for information about vertical sync.

Pins 8, 32 and 40 – V_{SUP} Supply Voltage
These pins must be connected to the positive of the supply.

Pins 9 to 15 – V6 to V0 Video Inputs (Fig. 2-3)
Via these pins, the DPU receives the digitized composite video signal from the VCU 2133 or VCU 2134 Video Codec in a parallel 7-bit Gray code. With a standard signal, the sync pulse resolution is 6 bits.

Pins 16 to 18 – IM Bus Connections
These pins connect the DPU to the IM bus. It is via the IM bus that the DPU communicates with the CCU. Pins 16 (IM Bus Clock Input) and 17 (IM Bus Ident Input) have the configuration shown in Fig. 2-2. Pin 18 (IM Bus Data Input/Output) is shown in Fig. 2-9.

Pin 19 – Combined Output for the Color Key Pulse and the Undelayed Horizontal Blanking Pulse (Fig. 2-11)
This output is tristate-controlled. In conjunction with the input load represented by the VCU, the three-level key and blanking pulse is produced which is also needed by the other DIGIT 2000 processors.

Pin 22 – Combined Output for the Delayed Horizontal Blanking Pulse and the Vertical Blanking Pulse (Fig. 2-11)
This pin is a tristate-controlled output. In conjunction with the input load represented by the VCU, the three-level combined blanking pulse is produced which is also needed by the other DIGIT 2000 processors.

Pin 23 – Horizontal Flyback Input (Fig. 2-5)
Pin 23 requires horizontal flyback pulses which must be clamped by a diode to the +5 V supply.

Pin 24 – Undelayed Horizontal Blanking Output (Fig. 2-11)
This output supplies undelayed horizontal blanking pulses. These pulses are for keying of the IF amplifier and are keying pulses for the VCU.

Pin 25 – Vertical Flyback Safety Input (Fig. 2-5)
To protect the picture tube from damage by burn-in in the event of a malfunction of the vertical deflection, an acknowledge pulse derived from the vertical deflection yoke is fed to pin 25. If this pulse exceeds the 2.5 V threshold during vertical blanking, the blanking pulse will be terminated. If it is planned to operate without this picture tube protection, pin 25 must be connected to +5 V.

Pin 26 – Vertical Flyback Output (Fig. 2-12)
This pin supplies the same pulsewidth-modulated sawtooth signal as pin 27, but only for 350 µs from the start of the vertical flyback. During the remaining time, pin 26 is at high impedance. The signal supplied by pin 26 is used for fast charge-reversal of the integration capacitor.

Pin 27 – Vertical Sawtooth Output (Fig. 2-12)
This pin supplies the signal, in pulsewidth-modulated form, for driving the vertical output stage. To produce the analog sawtooth signal, this signal must be integrated externally, e. g. by an RC network. By way of the IM bus interface and the HSP processor, it is possible for this sawtooth to be varied by the CCU.

Pin 28 – East-West Parabola Output (Fig. 2-12)
This pin supplies the vertical-frequency parabola signal for the east-west correction in pulsewidth-modulated form. Via the IM bus and the HSP processor, the east-west parabola can be adjusted by the CCU.

Pin 29 – Horizontal Output Polarity and Pulsewidth Select Input (Fig. 2-6)
This pin serves for selecting the polarity and the pulsewidth of the output pulses of pin 31 as described in section 3.4. This pin must be connected to ground or to +5 V.

Pin 31 – Horizontal Output (Fig. 2-10)
This output supplies the driving pulses for the horizontal output stage. The output pulse polarity can be selected by means of pin 29.

Pin 33 – External Standard Selection Input (Fig. 2-7)
This input is used for selecting the horizontal frequency standard, as shown in Table 3-2. If pin 33 is +5 V, the DPU operates only with the NTSC standard. If it is connected to ground, however, the DPU is set for the PAL or SECAM standard, and the horizontal standard can only be changed by the CCU command between PAL/SECAM and Text display mode. If pin 33 is unconnected, all standards can be selected by the CCU via the IM bus. Furthermore, when pin 33 is unconnected, the horizontal protection circuit is in effect, and for this a 4 MHz signal is required at pin 34. In this case, the output pulse at pin 31 is limited to a maximum duration of 30 µs for all standards. The phase resolution of the trailing edge of this pulse is reduced to 250 ns, if the output pulse is set to more than 30 µs pulsewidth.

Pin 34 – Protection Circuit Clock Input (Fig. 2-8)
When pin 33 is left unconnected, a 4 MHz clock signal is required at pin 34 for the horizontal protection circuit. The 4 MHz clock can be fed to pin 34 via a capacitor, and is available, e. g., at pin 1 of the CCU at no added cost. If the 4 MHz signal is not present and pin 33 is not connected, the horizontal output pin 31 is undefined.

Pin 35 – Start Oscillator Supply
Via this pin it is possible with minimum current consumption to operate the horizontal protection circuit as a starting oscillator. For this purpose only the 4 MHz signal at pin 34 is required. Pin 36 must be connected to pin 35.

Pin 36 – Start Oscillator Select Input (Fig. 2-6)
If the start oscillator function is required (see Table 3-2), pin 36 must be connected to pin 35. If the start oscillator function is not used, pin 36 has to be connected to ground. In this mode, the horizontal output pin 31 is switched off (at high level) as long as the $\overline{\text{Reset}}$ input pin 5 is Low.

Pin 37 – Control Switch Output for the Horizontal Power Stage (Fig. 2-11)
This pin serves for switching over the horizontal output stage to another frequency.

Pin 38 – Test pin
This pin is an input/output of the type shown in Fig. 2-9. It is used for testing the DPU during production and should be left unconnected in normal operation.

Pin 39 – Interlace Control Output (Fig. 2-10)
This pin is for controlling an AC coupled vertical power stage for interlace-free mode.

2.4 Pin Circuits

The following figures schematically show the circuitry at the various pins. The integrated protection structures are not shown. The letter "E" means enhancement, the letter "D" depletion, and "S" stands for signal.

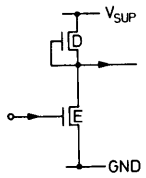


Fig. 2-2:
Input Pins 5, 16 and 17

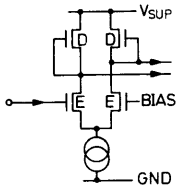


Fig. 2-3:
Input Pins 9 to 15

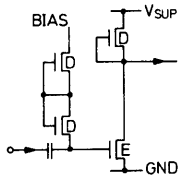


Fig. 2-4:
Input Pin 2

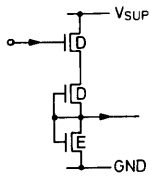


Fig. 2-5:
Input Pins 23 and 25

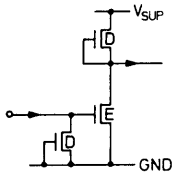


Fig. 2-6:
Input Pins 29 and 36

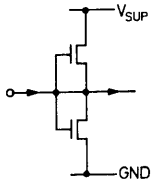


Fig. 2-7:
Input Pin 33

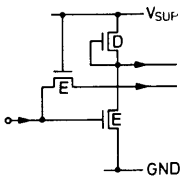


Fig. 2-8:
Input Pin 34

3. Functional Description

3.1. Block Diagram

The DPU 2553, DPU 2554 and DPU 2555 Deflection Processors perform all tasks associated with deflection in TV sets:

- sync separation
- generation and synchronization of the horizontal and the vertical deflection frequencies
- the various east-west corrections
- vertical sawtooth generation including S correction

as described hereafter. The DPU communicates, via the bidirectional serial IM bus, with the CCU 2030, CCU 2050 or CCU 2070 Central Control Unit and, via this bus, is supplied with the picture-correction alignment information stored in the MDA 2062 EEPROM during set production, when the set is turned on. The DPU is normally clocked with a trapezoidal 17.734 MHz (PAL or SECAM), or 14.3 MHz (NTSC) or 20.25 MHz (D2-MAC) clock signal supplied by the MCU 2600 or MCU 2632 Clock Generator IC. The functional diagram of the DPU is shown in Fig. 3-1.

3.2. The Video Clamping Circuit and the Sync Pulse Separation Circuit

The digitized composite video signal delivered as a 7-bit parallel signal by the VCU 2133 or VCU 2134 Video Codec is first noise-filtered by a 1 MHz digital lowpass filter and, to improve the noise immunity of the clamping circuit, is additionally filtered by a 0.2 MHz lowpass filter before being routed to theminimum and back porch level detectors (Fig. 3-2).

The DPU has two different clamping outputs, No. 1 and No. 2, one of which supplies the required clamping pulses to the video input of the VCU as shown in Fig. 3-1. The following values for the clamping circuit apply for Video Amp. I. Since the gain of Video Amp. II is twice that of Video Amp I, all clamping and signal levels of Video Amp II are half those of Video Amp I referred to +5 V.

After the TV set is switched on, the video clamping circuit first of all ensures by means of horizontal-frequency current pulses from the clamping output of the DPU to the coupling capacitor of the analog composite video signal, that the video signal at the VCU's input is optimally biased for the operation range of the A/D converter of 5 to 7 V. For this, the sync top level is digitally measured and set to a constant level of 5.125 V by these current pulses. The horizontal and vertical sync pulses are now separated by a fixed separation level of 5.250 V so that the horizontal synchronization can lock to the correct phase (see section 3.3. and Figs. 2-17 and 3-2).

With the color key pulse which is now present in synchronism with the composite video signal, the video clamping circuit measures the DC voltage level of the porch and by means of the pulses from pin 21 (or pin 4), sets the DC level of the porch at a constant 5.5 V (5.25 V for Video Amp II). This level is also the reference black level for the VPU 2203, CVPU 2233 or CVPU 2235 Video Processors.

When horizontal synchronization is achieved, the slice level for the sync pulses is set to 50 % of the sync pulse amplitude by averaging sync top and black level. This ensures optimum pulse separation, even with small sync pulse amplitudes (see application notes, section 4.).

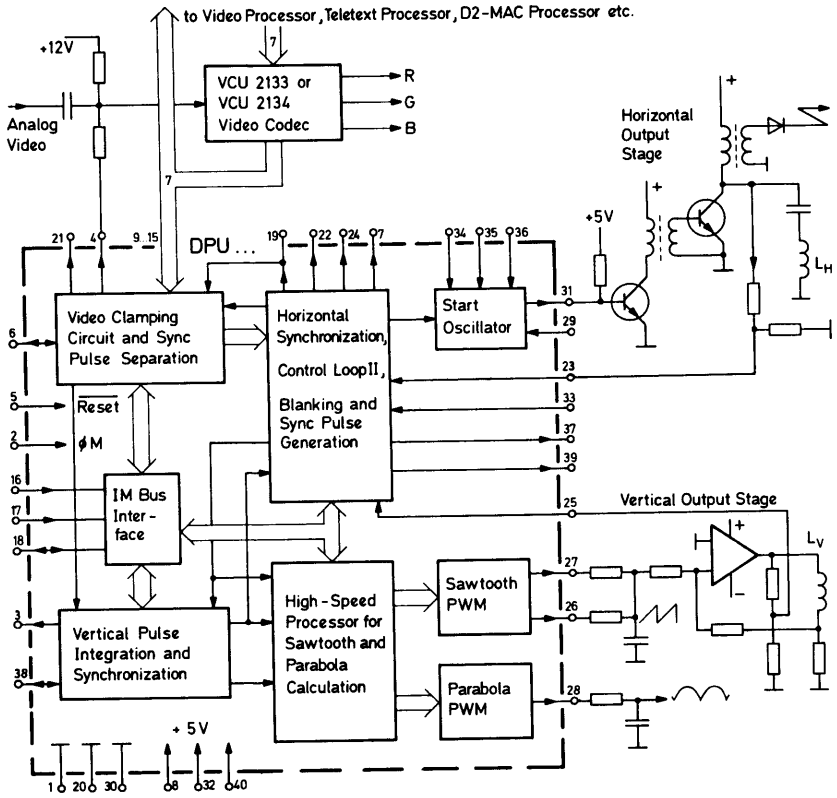
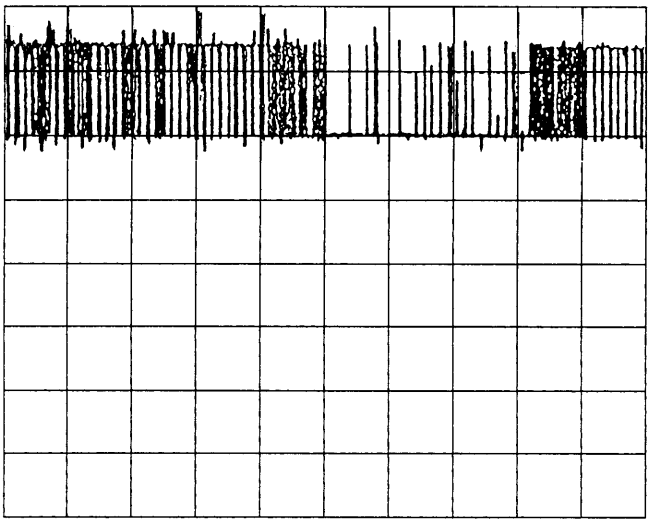


Fig. 3-1: Block diagram of the DPU 2553/54/55 Deflection Processors

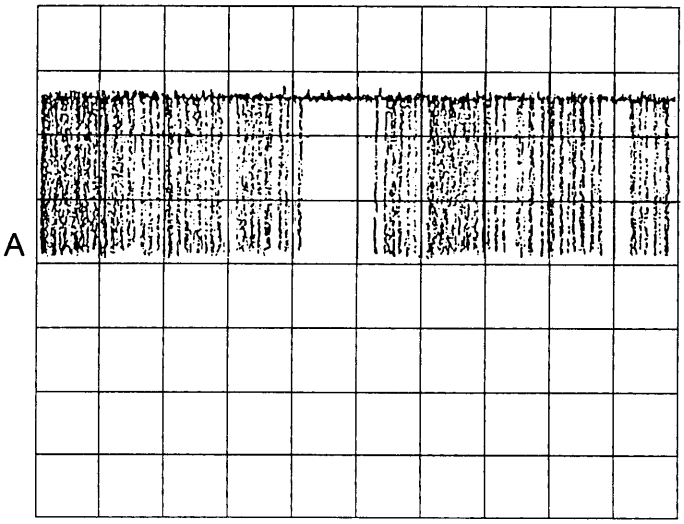
DPU 2553

PIN 9–15



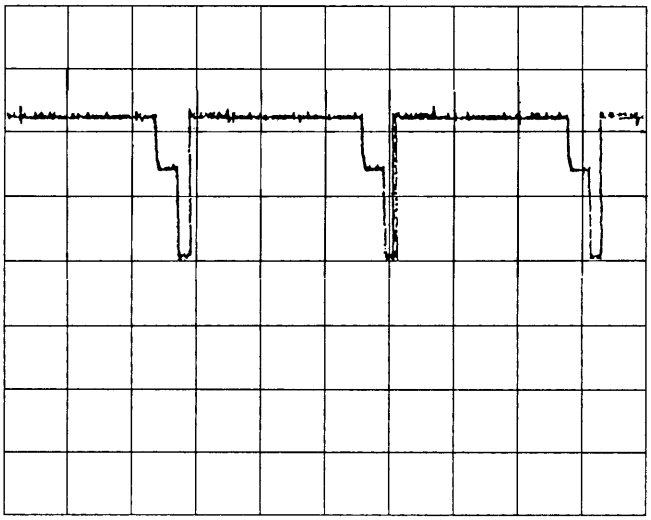
TIMEBASE 2 msec/div display 1/4
AMPL. 2 V/cm DC

PIN 16/17/18



TIMEBASE 100 µsec/div
AMPL. 2 V/cm DC

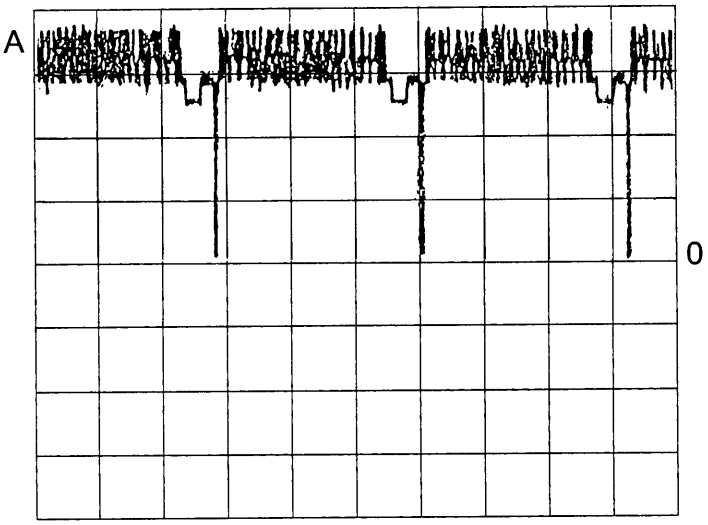
PIN 19



TIMEBASE 20 µsec/div
AMPL. 2 V/cm DC

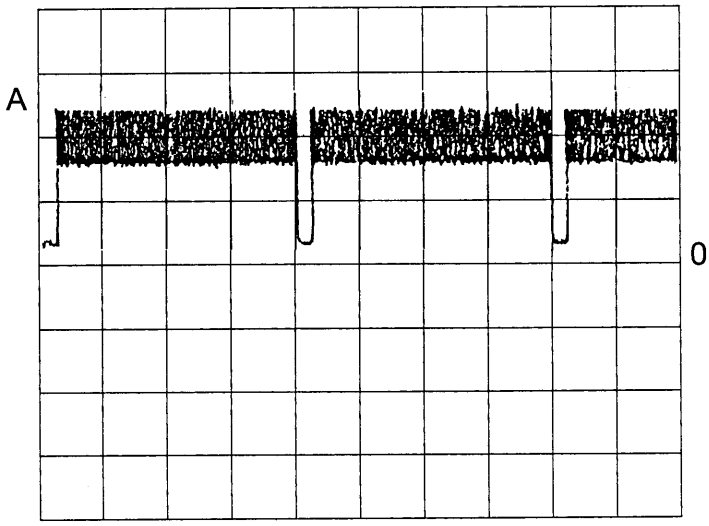
DPU

PIN 21



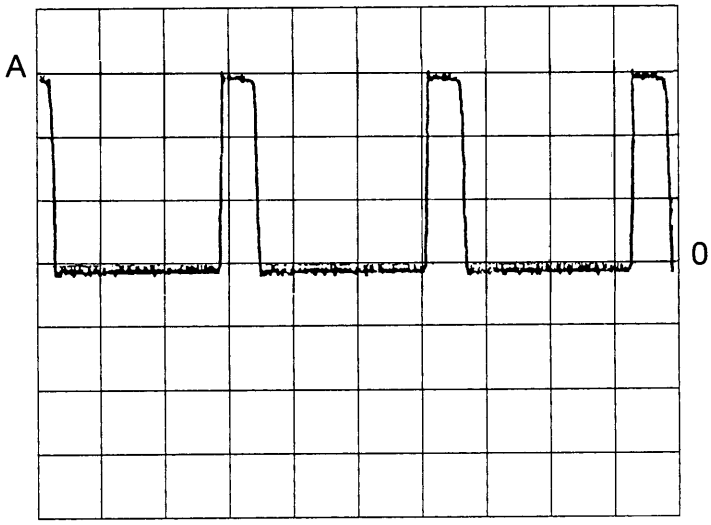
TIMEBASE 20 µsec/div
AMPL. 2 V/cm DC

PIN 22



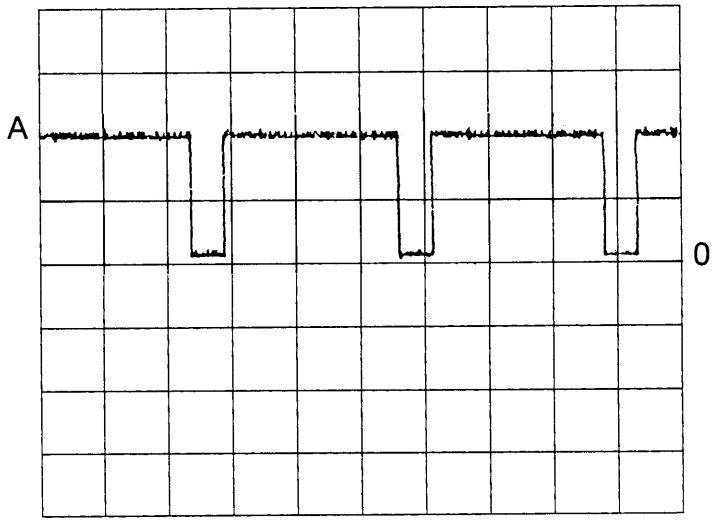
TIMEBASE 5 msec/div
AMPL. 2 V/cm DC

PIN 23



TIMEBASE 20 µsec/div
AMPL. 2 V/cm DC

PIN 24



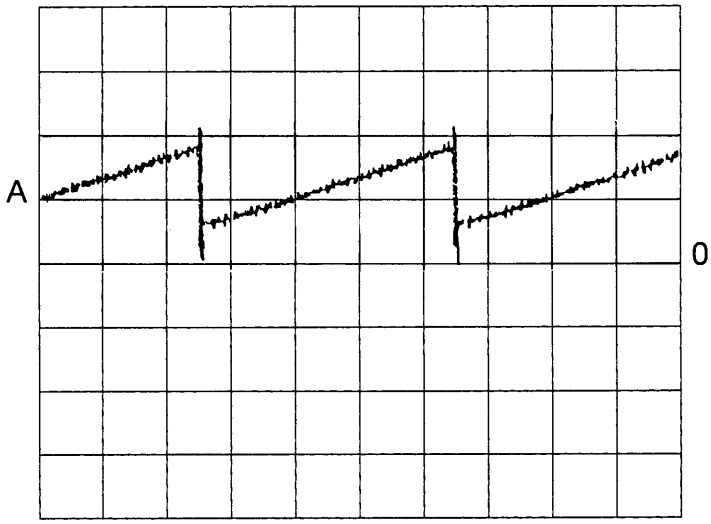
TIMEBASE 20 µsec/div
AMPL. 2 V/cm DC

DPU

PIN 25

TIMEBASE 5 msec/div
AMPL. 2 V/cm DC

PIN 26

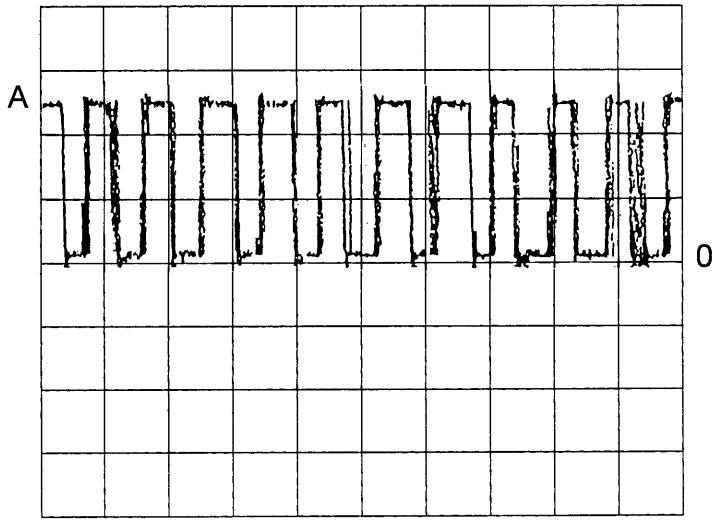


TIMEBASE 5 msec/div
AMPL. 2 V/cm DC

PIN 27

TIMEBASE 1 µsec/div
AMPL. 2 V/cm DC

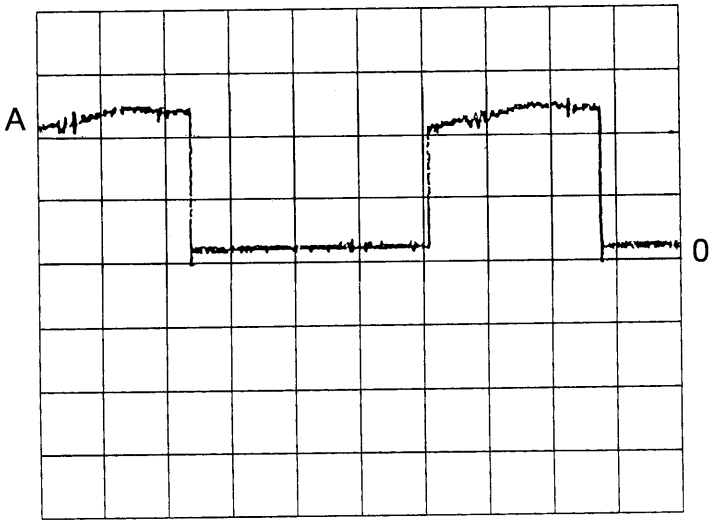
PIN 28



TIMEBASE 1 µsec/div
AMPL. 2 V/cm DC

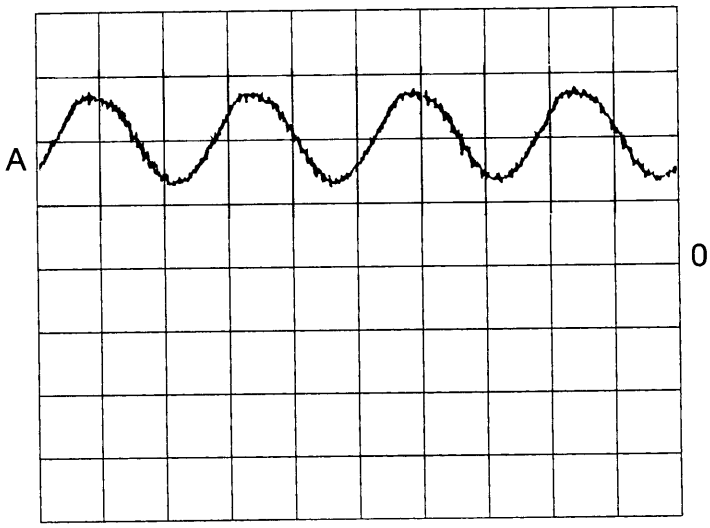
DPU

PIN 31



TIMEBASE 10 µsec/div
AMPL. 2 V/cm DC

PIN 34



TIMEBASE .1 µsec/div
AMPL. 1 V/cm DC

SPU 2220
SECAM Chroma Processor

SECAM Chroma Processor

Digital realtime signal processor for processing SECAM video chroma signals in combination with the VPU 2203 Video Processor which processes the luminance information at the same time.

The SPU 2220 is an N-channel VLSI MOS circuit, housed in a 40-pin Dil plastic package and contains on a single silicon chip the following functions:

- a code converter
- a digital SECAM bell filter
- a switchable IF spectrum compensation filter
- a digital FM demodulator with DC offset correction, deemphasis and demultiplexer
- a digital Red-/Blue-line identification
- a digital standard recognition circuit
- a color saturation multiplier with multiplexer for the color difference signals
- the IM bus interface circuit which provides the communication with the CCU 2030, CCU 2050 or CCU 2070 Central Control Unit via the bidirectional IM bus
- chroma outputs (pins 23 to 26) can be disabled by means of pin 22

1. Functional Description

The SPU 2220 digitally processes the SECAM color signals supplied in digital form as a parallel 7-bit Gray-coded signal by the VCU 2133 Video Codec. Acting in parallel with the VPU 2203 Video Processor (Fig. 2), the SPU 2220 separates the color information from the digital video signal, performs the bell filter function and the IF spectral compensation before submitting the 17.734 MHz sampled signal to the digital algebraic demodulator.

The demodulator produces an 8-bit signal, sampled at 4.43 MHz, whose amplitude is proportional to the frequency of the incoming frequency-modulated color difference signal. After demodulation, the color difference signals undergo digital de-emphasis before being demultiplexed using a 64 µs delay line. After passing the saturation multiplier the color difference signals are multiplexed in a form compatible to that used in the VPU 2203.

The SPU 2220 also includes automatic SECAM identification logic as well as Red-/Blue-Line detection and synchronization. Since the signal-processing delay in the performance of SECAM decoding is greater than that experienced during PAL or NTSC decoding, the SPU 2220 compensates for this delay by delaying the digital video signal supplied to the VPU 2203 by a corresponding amount (5.5 µs) in SECAM operation.

1.1. The Code Converter

The 7-bit digital video signal supplied by the VCU 2133 Video Codec in the Gray code is initially converted into 7-bit two's complement binary code for further processing.

1.2. The 5.5 µs Delay Line

This part of the SPU 2220 delays the digital video signal supplied by the VCU 2133 to be delivered to the VPU 2203. In this way the difference in processing time between the VPU 2203 (luminance channel) and the SPU 2220 (chrominance channel) in SECAM operation is compensated. The color key pulse for the VPU 2203 passes the Aux Delay block of the SPU 2220 in order to provide the same delay as for the video signal delayed in the 5.5 µs delay line.

1.3. The SECAM Bell Filter

This filter which has the same function as the conventional LC bell filter hitherto used, removes the luminance information and compensates the anti-bell response of the transmitter. Center frequency and frequency response of the bell filter are fixed and cannot be altered externally. The response of the SECAM bell filter is shown in Figs. 3 and 4.

1.4. The IF Spectrum Compensation Filter

Since the FM color information in the SECAM system covers a range of frequencies from 3.9 to 4.75 MHz (unlike the single frequency with its AM color information in the PAL and NTSC systems), the slight spectral distortion resulting from the tuner and IF section of the TV set should be compensated. For this, the 14-bit output of the bell filter passes the IF spectrum compensation filter which gives a compensating frequency response of about 4 dB/MHz.

This filter can be switched on and off by the CCU via the IM bus using address 107 (see Table 2). Fig. 4 shows the various filter responses of the bell and IF compensation filter with the latter switched on and off.

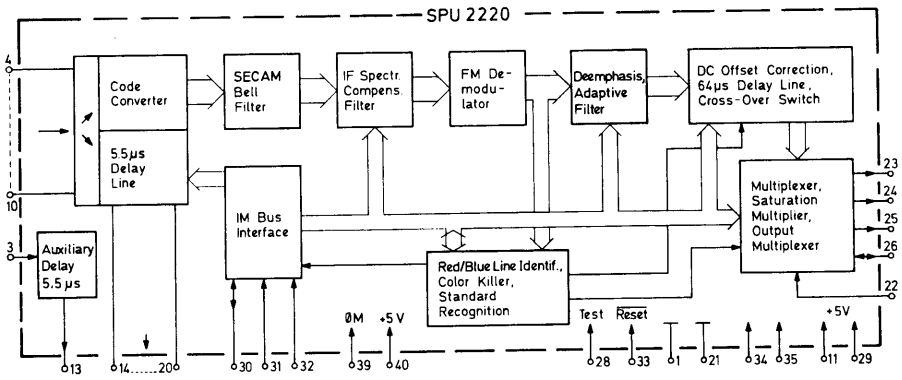


Fig. 1: Block diagram of the SPU 2220

2. Outline Dimensions and Pin Connections

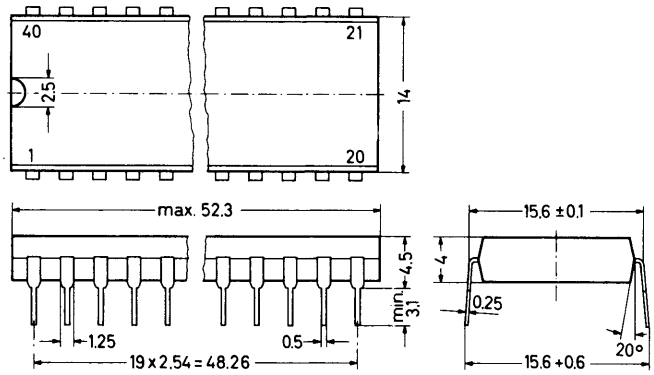


Fig. 8:
SPU 2220 in 40-pin Dil Plastic Package,
20 B 40 according to DIN 41 870

Weight approx. 6 g Dimensions in mm

Pin connections (preliminary information, subject to modifications)

1	Ground, 0
2	NC
3	Aux Delay In
4	V0 Video Input (LSB)
5	V1 Video Input
6	V2 Video Input
7	V3 Video Input
8	V4 Video Input
9	V5 Video Input
10	V6 Video Input (MSB)
11	V_{SUP} Supply Voltage
12	NC
13	Aux Delay Out
14	DV0 Delayed Video Output (LSB)
15	DV1 Delayed Video Output
16	DV2 Delayed Video Output
17	DV3 Delayed Video Output
18	DV4 Delayed Video Output
19	DV5 Delayed Video Output
20	DV6 Delayed Video Output (MSB)
21	Ground, 0
22	Outputs Disable Input
23	C3 Chroma Output (MSB)
24	C2 Chroma Output
25	C1 Chroma Output
26	C0 Chroma Output (LSB), Msync Input
27	Test Output P4
28	Test Input
29	V_{SUP} Supply Voltage
30	IM Bus Data Input/Output
31	IM Bus Ident Input
32	IM Bus Clock Input
33	$\overline{\text{Reset}}$ Input
34	Undelayed Horizontal Blanking Input
35	Vertical Blanking Input
36	NC
37	NC
38	NC
39	ØM Main Clock Input
40	V_{SUP} Supply Voltage

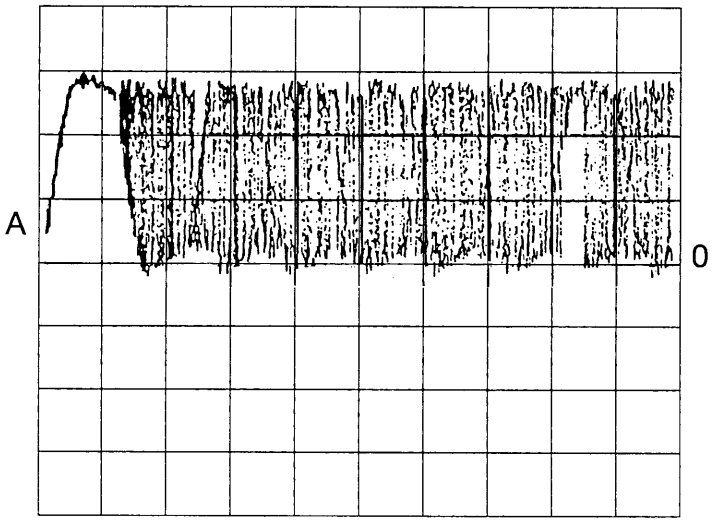
3. Electrical Characteristics

All voltages are referred to pins 1 and 21.

Absolute Maximum Ratings

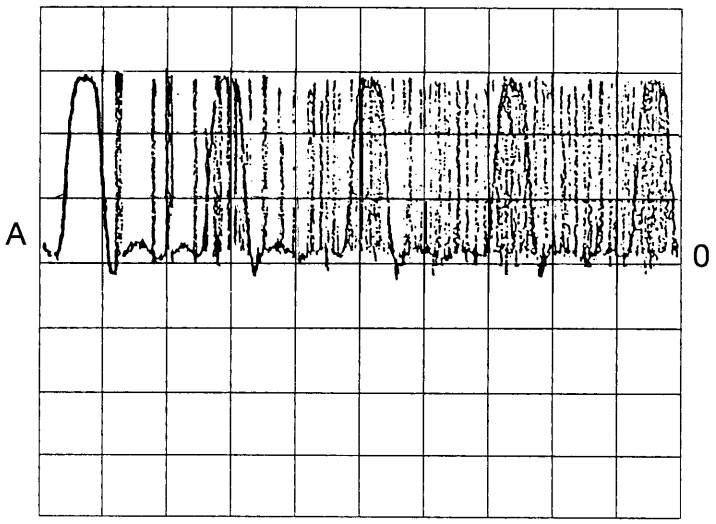
	Symbol	Value	Unit
Supply Voltage, Pins 11, 29 and 40	V_{SUP}	6	V
Output Current, all Outputs	I_D	10	mA
Output Voltage, all Outputs	V_D	−0.3 V to V_{SUP}	–
Input Voltage, all Inputs	V_I	−0.3 V to V_{SUP}	–
Ambient Operating Temperature Range	T_A	0 to +65	°C
Storage Temperature Range	T_S	−40 to +125	°C

PIN 14–18



TIMEBASE .2 µsec/div display 1/4
AMPL. 2 V/cm DC

PIN 19/20



TIMEBASE .1 µsec/div
AMPL. 2 V/cm DC

CVPU 2233
NTSC Comb Filter
Video Processor

NTSC Comb Filter Video Processor

Digital real-time signal processor for processing the video signals digitized by the VCU 2133 Video Codec Unit in digital color TV receivers according to the NTSC standard. The CVPU 2233 is an N-channel MOS circuit, is housed in a 40-pin Dil plastic package and contains on a single silicon chip the following functions:

- a code converter
- an NTSC comb filter
- the chroma bandpass filter
- the luminance filter with peaking facility
- a contrast multiplier with limiter for the luminance signal
- all color signal processing circuits such as automatic color control (ACC), color killer, identification, decoder and hue correction
- a color saturation multiplier with multiplexer for the color difference signals
- the IM bus interface circuit for communicating with the CCU 2030 or CCU 2050 Central Control Unit
- circuitry for measuring dark current (CRT spot-cutoff), white level and photo current, and for transferring this data to the CCU.

1. Functional Description

The CVPU 2233 Comb Filter Video Processor digitally processes the digital video signal supplied by the VCU 2133 Video Codec in the various circuit parts just mentioned. The resulting digital signals are then reconverted to analog signals in the VCU 2133 and used to drive the cathodes of the picture tube, via the external RGB output amplifiers. Further, in conjunction with the VCU 2133, the CVPU 2233 performs a number of measurements and control operations relating to picture tube alignment such as spot-cutoff current adjustment, white level control, beam current limiting, etc.

To understand the signal processing in the two integrated circuits VCU 2133 and CVPU 2233, Fig. 2 may prove useful because it shows the signal flow and the several functional blocks in their logical sequence regardless of whether these blocks are in the VCU 2133 or CVPU 2233.

1.1. The Code Converter

This circuit is shown only in Fig. 1. It serves to convert the digitized video signal, delivered by the VCU 2133 in a parallel Gray code, into a simple binary-coded signal for the comb filter.

1.2. The Comb Filter

With the NTSC system, a comb filtering for separation of chrominance and luminance signals is easy to realize by a delay line that has the delay of one horizontal period (64 µs). In the case of the CVPU 2233, this delay is realized by a RAM. When a comb filter is used, it is no longer necessary to have a chroma trap in the luminance signal path.

1.3. The Luminance Channel

The luminance filter has two different values for its bandwith, 4 MHz in the case an IF filtered video signal is processed, and 7 MHz if the video signal originates from a camera, a video signal disc player etc. Additionally, the filter handles peaking whereby the high-frequency components of the luminance signal in the range of 3 MHz are raised to improve picture sharpness. The amount of peaking is set by the CCU 2030 or CCU 2050 via the IM bus. Using a fixed subtrahend of −0.25, the sync signal component not required in the luminance channel is suppressed. Peaking at 3 MHz is provided in the range from −3 dB to + 10 dB. It can be set by the user in eight steps. The peaking has a dead-data zone as shown in Fig. 14 in the description of the VCU 2133.

The luminance filter has a DC gain of 1.0 (see Fig. 4). Behind the luminance filter, 9 bits are used to carry the luminance signal, so that the overshoots caused by the peaking filter can be transmitted to the Y D/A converter in the VCU 2133. The peaking curves are shown in Fig. 5.

Following the peaking circuit (Fig. 2) is the contrast multiplier which, combined with a limiter, limits the luminance signal if its amplitude becomes too high. The contrast setting, too, is controlled by the CCU via the IM bus, depending on the user's instructions. Further, the contrast is adapted to the room lighting by means of a photo sensor

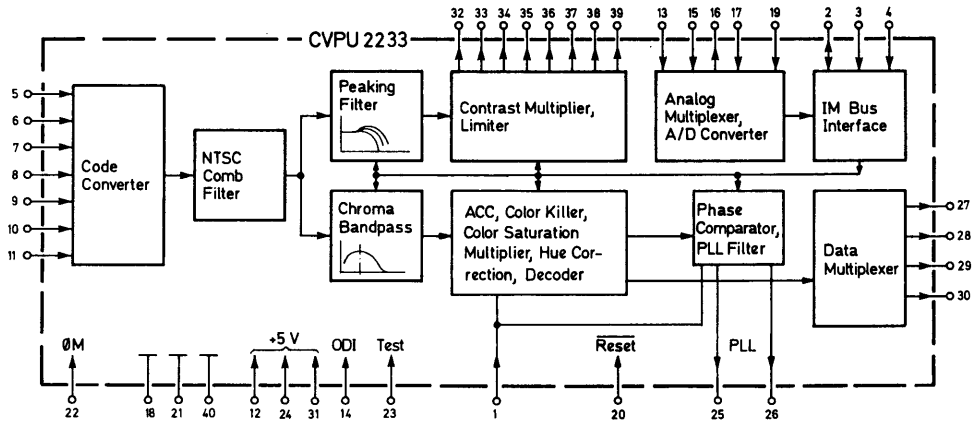


Fig. 1: Block diagram of the CVPU 2233 Comb Filter Video Processor

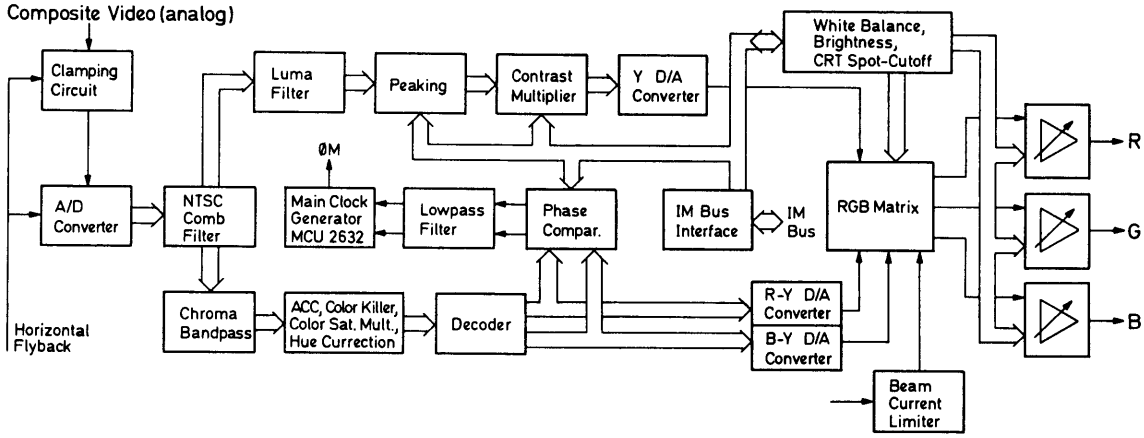


Fig. 2: Block diagram of the VCU 2133 and CVPU 2233 combination taking into account the sequence of the signal flow

connected to pin 17 of the CVPU 2233. In this process, the signal generated by the photo sensor is first digitized in the CVPU 2233 and then, during vertical flyback, transferred in multiplex operation to the CCU. The CCU calculates the contrast needed and finally sends the corresponding control signal to the CVPU 2233's contrast multiplier via the IM bus. After the contrast multiplier are added 31 steps as a constant DC signal, so that the system can transmit the negative undershoots caused by peaking, to the D/A converter (see Fig. 3).

From the contrast multiplier, the digital luminance signal is fed back to the VCU 2133 in the form of a 8-bit signal. In the VCU 2133, the signal enters the Y D/A converter. The converter feeds the analog luminance signal to the RGB matrix.

The setting range of the contrast multiplier comprises 6 bits (63 steps) and a gain of 1. If the product of the multiplication at the multiplier's output is higher than the working range, the largest possible number (1 1 1 1 1 1 1 1) is put out. This means the limiting mentioned above is achieved.

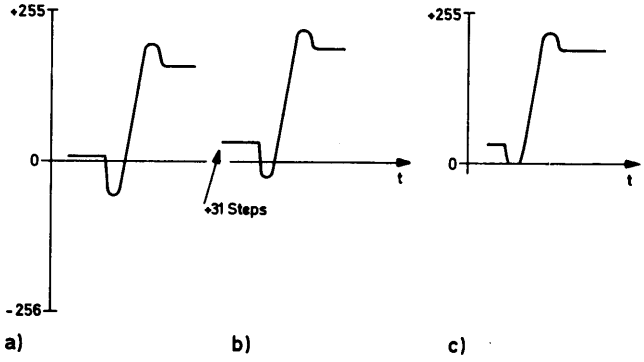


Fig. 3: Adding 31 steps DC signal
a) peaked signal after filter
b) the same signal with added 31 steps, this means a constant DC level or brightness
c) the signal at the output of the luminance D/A converter

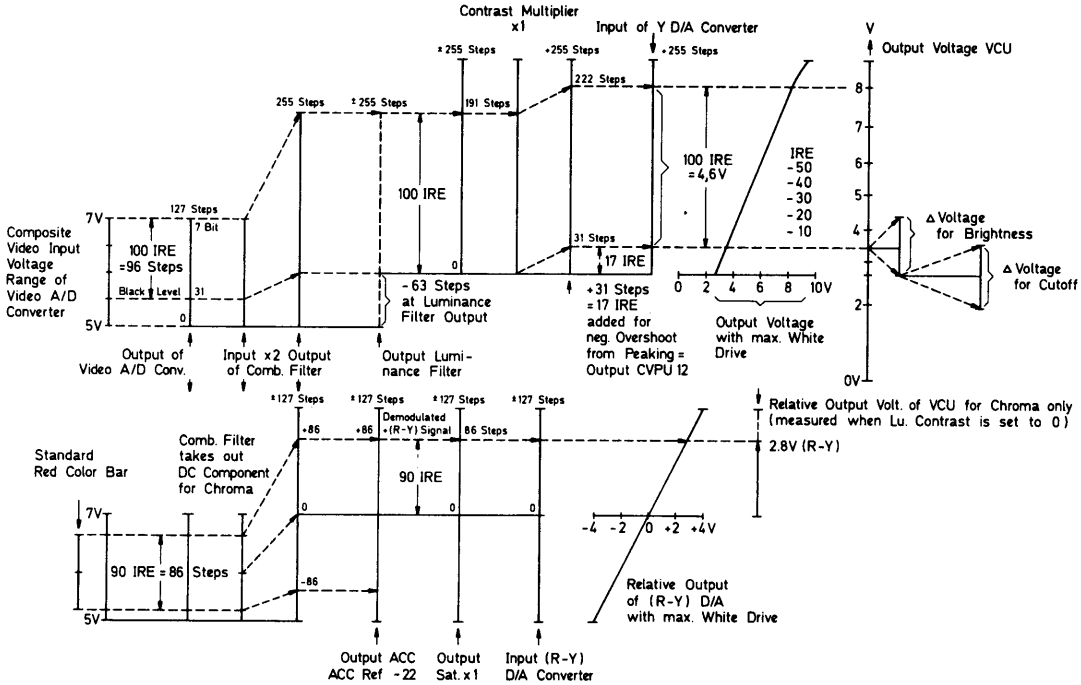


Fig. 4: Luminance and Chrominance Level Diagram applicable for the combination of VCU 2133 and CVPU 2233

continued notes to Table 3:

(q) The CCU must send a 16-bit word to CVPU
(r) Bit r = 1: when operating with the DMA D2-MAC Decoder, the adding of a step of ½ LSB (every other line) to the output signal of the Y A/D converters in the VCU 2133 is switched off.
(s) Bit s = 1: the blanking pulse in the analog video output signals at pins 26 to 28 of the VCU 2133 is switched off (required in stand-alone applications).
(t) Bit p = 1: the gain doubling of the VCU's input amplifier during the undelayed horizontal blanking pulse is switched off.
(u) Bit q = 1: the bit enlargement by means of the A/D converter's reference voltage is switched off.

Table 4: Code bits from CVPU to CCU (Addr. 16 and 22)

A	B	Code Bits		
		R	G	B
0	0	1	1	1
1	0	0	1	1
0	1	1	0	1
1	1	1	1	0

2. Outline Dimensions and Pin Connections

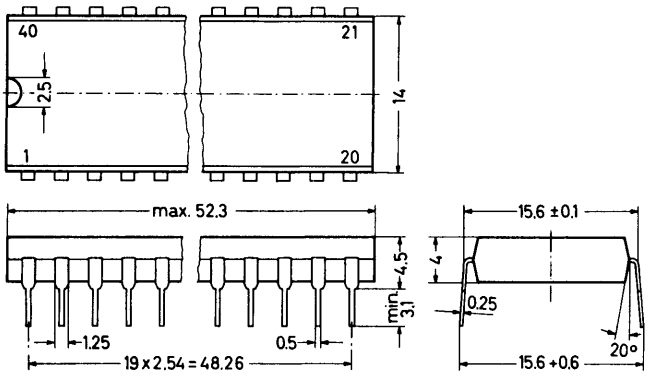


Fig. 8:
CVPU 2233 in 40-pin Dil Plastic Package,
20 B 40 according to DIN 41 870

Weight approx. 6 g Dimensions in mm

Table 5: Variable luminance delay (Address 15)

Bits of low Byte 7	6	5	4	Number of Clock cycles
0	1	1	1	+4
0	1	1	0	+3
0	1	0	1	+2
0	1	0	0	+1
1	×	×	×	0
0	0	1	1	−1
0	0	1	0	−2
0	0	0	1	−3
0	0	0	0	−4

Pin Connections

1	Color Key Pulse Input
2	IM Bus Data Input/Output
3	IM Bus Ident Input
4	IM Bus Clock Input
5	V0 Input (LSB)
6	V1 Input
7	V2 Input
8	V3 Input
9	V4 Input
10	V5 Input
11	V6 Input (MSB)
12	Supply Voltage, +5 V
13	Vertical Blanking Pulse Input
14	Outputs Disable Input
15	Beam Current Input
16	Beam Current Switchover Output
17	Photo Sensor Input
18	Analog Ground, 0
19	Reference Voltage Input
20	$\overline{\text{Reset}}$ Input
21	Digital Ground, 0
22	ØM Main Clock Input,
23	Test Pin, connect to GND
24	Supply Voltage, +5 V
25	Data Clock Output (PLL)
26	Data Output (PLL)
27	C0 and Msync Output (LSB)
28	C3 Output (MSB)
29	C2 Output
30	C1 Output
31	Supply Voltage, +5 V
32	L0 Output (LSB)
33	L1 Output
34	L2 Output
35	L3 Output
36	L4 Output
37	L5 Output
38	L6 Output
39	L7 Output (MSB)
40	Digital Ground, 0

4. Inner Configuration of the Connection Pins

The following figures schematically show the circuitry at the various pins. The integrated protection structures are not shown. The letter "E" means enhancement, the letter "D" depletion.

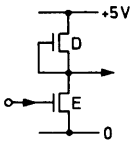


Fig. 8:
Pins 1, 3, 4, 13, 14 and 20, Inputs

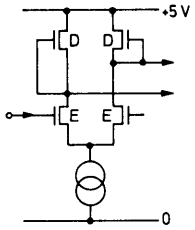


Fig. 9:
Pins 5 to 11, Inputs

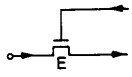


Fig. 10:
Pins 15 and 17, Inputs

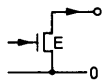


Fig. 11:
Pins 16, 25 to 30 and 32 to 39, Outputs

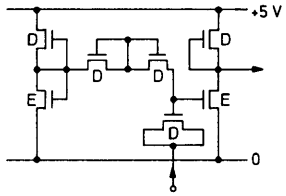


Fig. 12:
Pin 22, Input

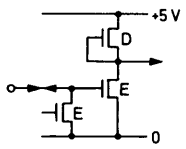


Fig. 13:
Pin 2, Input/Output

5. Description of the Connections and the Signals

Pin 1 – Color Key Pulse Input
This input's configuration is shown in Fig. 8. Via this pin, the CVPU 2233 gets the color key pulse from pin 19 of the DPU 2543. In the quiescent state high level must be applied, and during pulse a low level.

Pins 2 to 4 – IM Bus Connections
By means of these pins, the CVPU 2233 is linked with the CCU 2030 or CCU 2050. Pins 3 (Ident Input) and 4 (Clock Input) are configured as shown in Fig. 8. Pin 2 (Data Input/ Output) is shown in Fig. 13.

Pins 5 to 11 – Inputs V0 to V6
The circuit of these inputs is shown in Fig. 9. Via these inputs, the CVPU 2233 receives the digitized composite video signal from the VCU 2133 in a 7-bit parallel Gray code. Input V0 gets the least significant bit (LSB) and input V6 the most significant bit (MSB).

Pins 12, 24 and 31 – Supply Voltage, +5 V
These pins must be connected to the positive of the 5 V supply.

Pin 13 – Vertical Blanking Pulse Input
Fig. 8 shows the diagram of this input. Via this pin the CVPU 2233 receives the vertical blanking pulse from the DPU 2543. In the steady state, high level must be applied, and during pulse a low level. The vertical blanking pulse is required for controlling the tests described in section 1.5., which are carried out during vertical flyback.

Pin 14 – Outputs Disable Input
This input (Fig. 8) serves for fast switchover of the luma and chroma outputs (Pin 27 to 30 and 32 to 39) to the high-impedance state. Pin 14 low means outputs active, and Pin 14 high means outputs disabled.

Pin 15 – Beam Current Input
By means of this pin, whose circuit is shown in Fig. 10, the CVPU 2233 receives the common analog signal which is supplied by three current sensing transistors inserted in the cathode lines of the picture tube. Via the internal switch S1 (Fig. 5) the analog signal is fed to the internal A/D converter. Input voltage range is 0 V to V_{19}.

Pin 16 – Beam Current Switchover Output
This pin serves for selecting the sensitivity of the beam current input pin 15 by connecting an additional 10 kΩ resistor parallel to pin 15 and ground, thus reducing this input's sensitivity. By this means, the current supplied by the three sensor transistors mentioned is the spot-cutoff current on the one hand (high sensitivity) and the white level current on the other (low sensitivity). The circuit of pin 16 is shown in Fig. 11.

Pin 17 – Photo Sensor Input
This input has the same properties as pin 15. It serves for measuring the current supplied by the photo sensor and is activated by switch S2 (Fig. 5). Its input voltage range is also 0 V to V_{19}.

Pin 18 – Analog Ground, 0
This pin is used as a ground connection in conjunction with pins 15 to 17.

Pin 19 – Reference Voltage Input
This pin gets the externally-produced reference voltage of half the supply voltage, that is required by the circuitry shown in Fig. 5 and must be filtered by a capacitor of sufficient capacity.

Pin 20 – $\overline{\text{Reset}}$ Input
This pin's circuit is shown in Fig. 8. In the steady state, high level is required. A low level normalizes the CVPU 2233.

Pins 21 and 40 – Digital Ground, 0
These pins are used as ground connection in all cases where digital signals are involved.

Pins 22 – ØM Main Clock Input
Via this pin the CVPU 2233 is supplied with the required main clock signal by the MCU 2600 or MCU 2632 Clock Generator IC. Fig. 12 shows the diagram of Pin 22.

Pin 23 – Test Pin
During normal operation, this pin must be connected to ground.

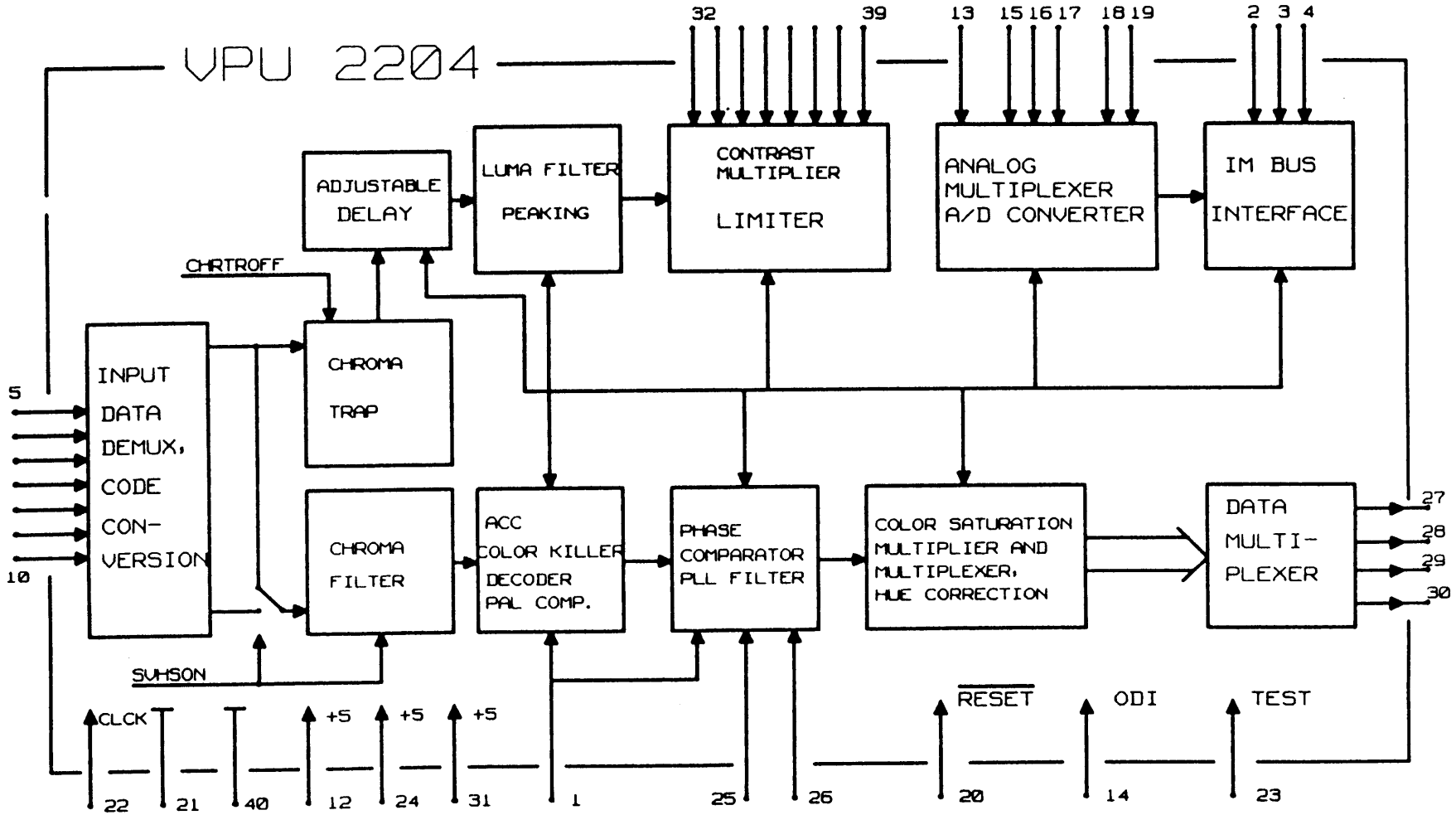
Pin 25 – Data Clock Output (PLL)
This pin whose diagram is shown in Fig. 11 supplies the data clock signal needed for the serial data transfer of the PLL information from the phase comparator contained in the CVPU 2233 to the voltage-controlled oscillator (VCO) contained in the MCU 2600 or MCU 2632 Clock Generator IC. The frequency of the data clock signal is one fourth of the main clock's frequency.

Pin 26 – Data Output (PLL)
This pin whose diagram is shown in Fig. 11 supplies the 12-bit data word explained in section 1.6., which serves for closing the PLL circuit which determines the main clock signal used in the DIGIT 2000 TV receiver.

Pins 27 to 30 – Outputs C3 to C0
These outputs' configuration is shown in Fig. 11. Via these pins, the R-Y, B-Y, and picture tube alignment data is transferred in multiplex operation to the VCU 2133.

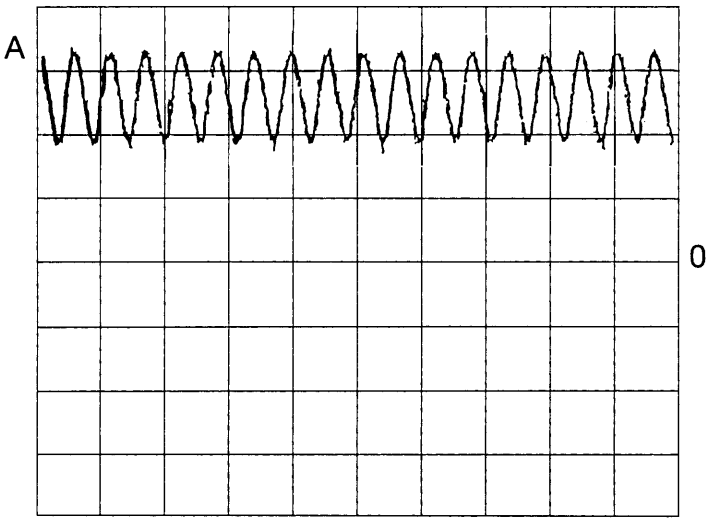
Pins 32 to 39 – Outputs L0 to L7
These outputs are identical to pin 27, too. Via these pins, the CVPU 2233 delivers the digital luminance signal (Y) to the VCU 2133, where it is reconverted to an analog signal.

VPU 2204


VPU 2204
32
39
13
15 16 17
18 19
2 3 4
ADJUSTABLE DELAY
LUMA FILTER PEAKING
CONTRAST MULTIPLIER LIMITER
ANALOG MULTIPLEXER A/D CONVERTER
IM BUS INTERFACE
CHRTROFF
INPUT DATA DEMUX, CODE CON-VERSION
CHROMA TRAP
CHROMA FILTER
ACC COLOR KILLER DECODER PAL COMP.
PHASE COMPARATOR PLL FILTER
COLOR SATURATION MULTIPLIER AND MULTIPLEXER, HUE CORRECTION
DATA MULTI-PLEXER
5
10
27
28
29
30
SVHSON
CLCK
+5
+5
+5
RESET
ODI
TEST
22
21
40
12
24
31
1
25
26
20
14
23

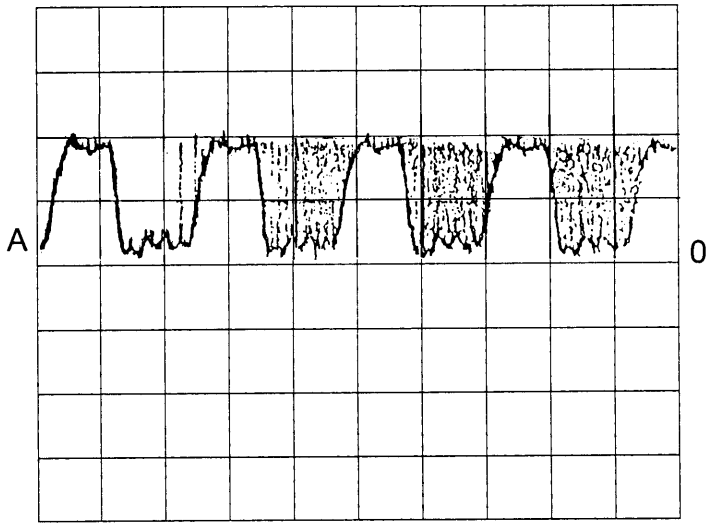
PVPU 2204

PIN 22



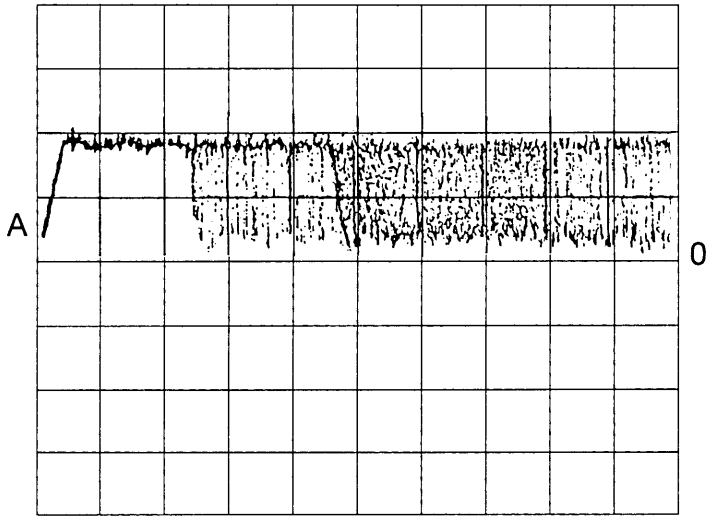
TIMEBASE .1 µsec/div
AMPL. 1 V/cm DC

PIN 25



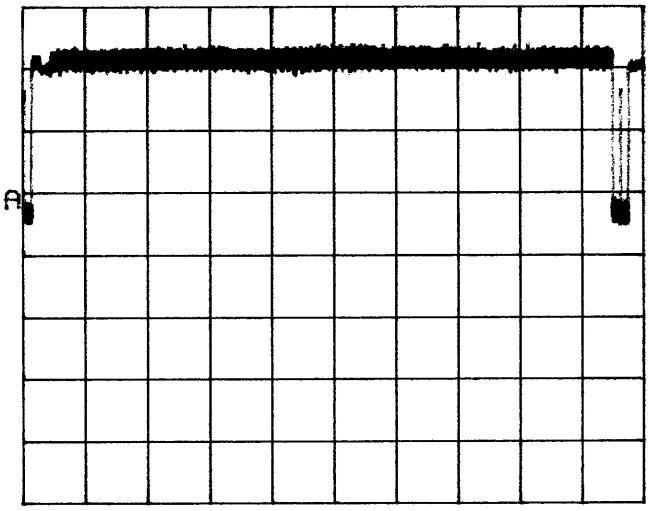
TIMEBASE .1 µsec/div
AMPL. 500 mV/cm DC

PIN 26



TIMEBASE .1 µsec/div
AMPL. 500 mV/cm DC

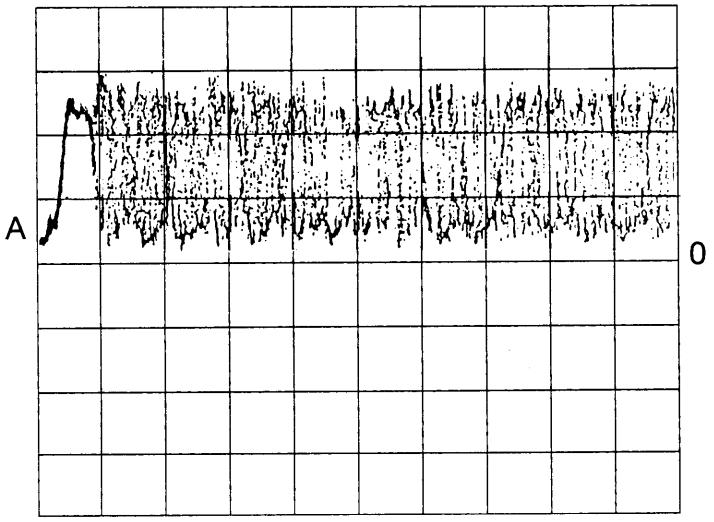
PIN 28, 29



TIMEBASE 2 msec/div
AMPL. 0.5 V/cm DC

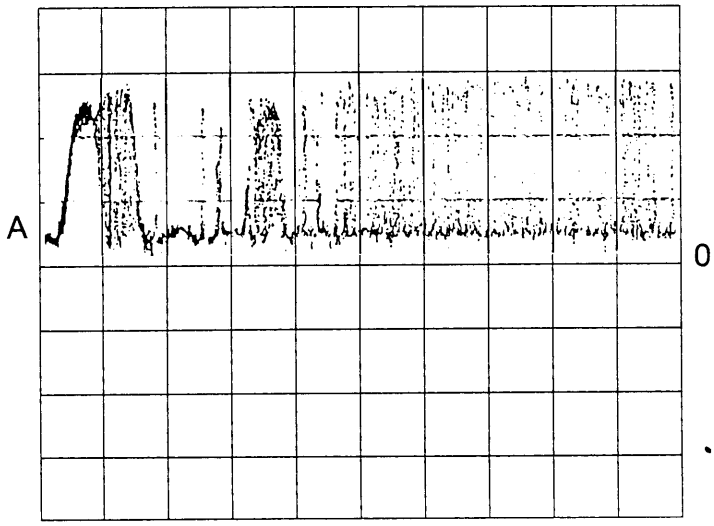
PVPU

PIN 27–30



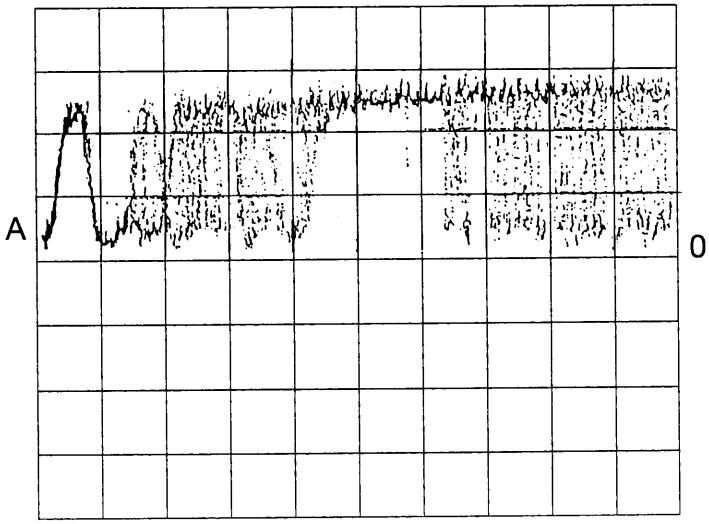
TIMEBASE .1 µsec/div
AMPL. 500 mV/cm DC

PIN 32–37/39



TIMEBASE .1 µsec/div
AMPL. 500 mV/cm DC

PIN 38



TIMEBASE .1 µsec/div
AMPL. 500 mV/cm DC

3. Functional Description

3.1. Block Diagram

The DTI 2222 is an N-channel MOS circuit which contains on one silicon chip mainly the following functional blocks (see Fig. 3-1):

- chroma nibble demultiplexer and R-Y/B-Y demultiplexer
- R-Y and B-Y interpolation filters
- R-Y and B-Y risetime detectors
- hold pulse generator
- chroma nibble multiplexer
- clock generator and MUX/DEMUX control
- luminance delay circuit
- IM bus interface

The normal risetime of luminance transients is about 150 ns, however, for chrominance transients the risetime is between 800 and 1000 ns. The picture impression, especially of color bars in the standard test pattern, is considerably improved if the chrominance transients are given the same short risetime as the luminance tran-

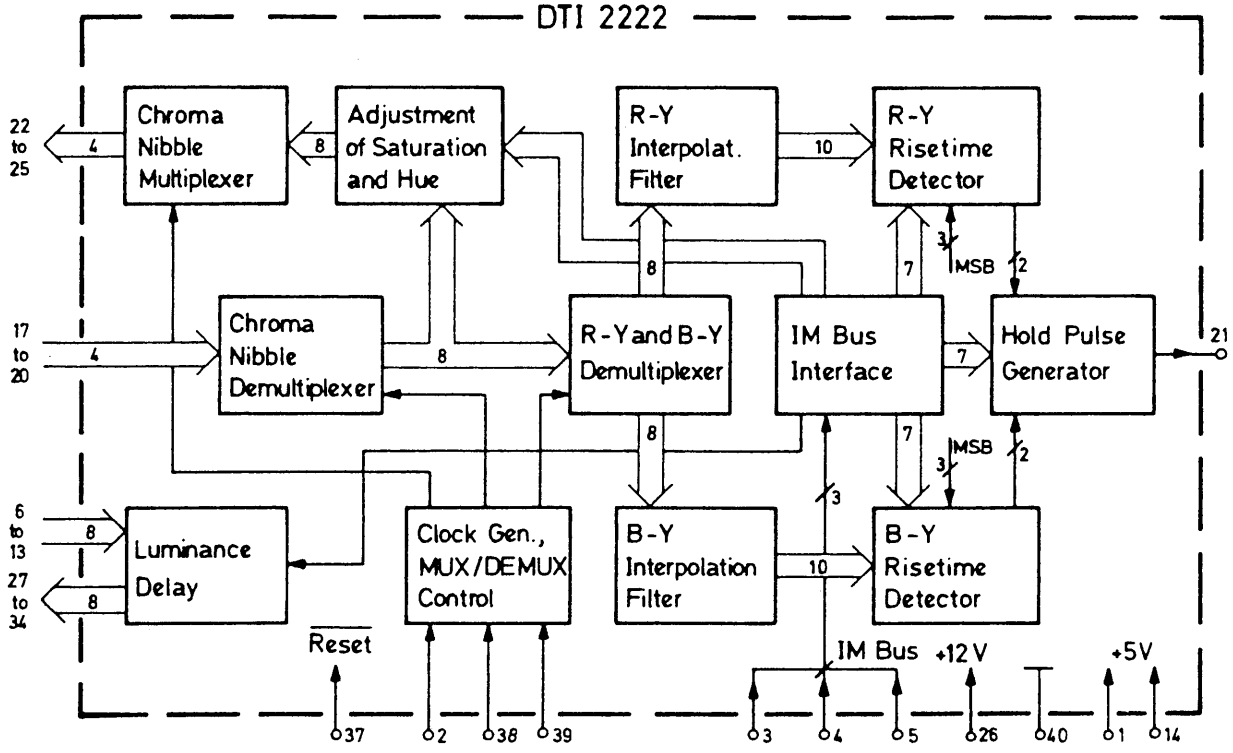


Fig. 3-1: DTI 2222 block diagram

Teletext Processor for Level 1 Teletext

The TPU 2732 is specified to handle Level-1-Teletext information (in Germany: Videotext) as it is transmitted today by the TV broadcast stations in Great Britain, Germany and other European countries. In this function, the TPU 2732 is part of the DIGIT 2000 digital TV system and works in conjunction with the other VLSI circuits and processors of this system. The Teletext adapter designed with the TPU 2732 is very simple and economic (Fig. 1), so that this new feature may now become common as it was not possible due to the high cost of former multi-chip solutions up to now.

The TPU 2732 is an N-channel VLSI MOS circuit, housed in a 40-pin Dil plastic package and contains on a single silicon chip the following functions:

- one-chip solution of the Teletext processing (except for external RAM)
- ghost compensation to eliminate the effects of ghost pictures due to reflections
- as input signal is used the 7-bit digitized composite video signal delivered in a parallel Gray code by the VCU 2133 or VCU 2134 Video Codec
- reduced access time is provided for the Teletext pages by receiving and storing up to eight pages in one go
- up to eight stored pages
- function extended by automatic language-dependent character selection
- switchover facility PAL/NTSC

TPU 2732 H for Hebrew Characters

Using the type designation TPU 2732 H, a mask option of the TPU 2732 can be supplied which, instead of the automatic language-dependent character selection described in sections 9.7. and 10.3., only displays the Hebrew character set. With this device, the language-selecting control bits C_{12} to C_{14} or LS0 to LS2 have no effect.

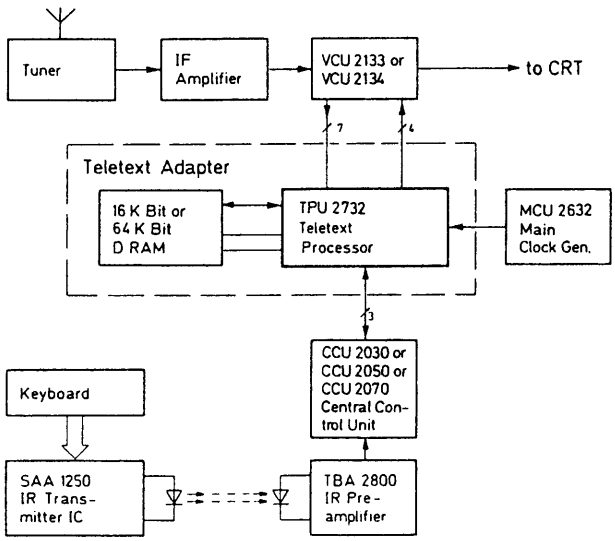


Fig. 1: Teletext application block diagram

1. Short Functional Description

The TPU 2732 whose block diagram is shown in Fig. 2, operates according to a rigid timing determined by the vertical cycle of the TV receiver. The data acquisition period starts at line 7 with PAL or line 10 with NTSC and ends at line 22 with PAL or line 21 with NTSC. During this period, the input data is processed by a ghost filter which is able to compensate reflections with short delay time of 0 to 0.8 µs for PAL or 0 to 1 µs for NTSC.

Teletext information is synchronized and identified. A comparator preselects the pages with page numbers that are requested by the CCU 2030, CCU 2050 or CCU 2070 Central Control Unit and loads them into the RAM. To eliminate speed problems of the external RAMs, the data is buffered in an internal RAM buffer (Fig. 2). The comparator contained in the data acquisition unit decides into which sector of the RAM the data is stored.

The display period starts at line 48 with PAL or line 50 with NTSC and ends at line 286 with PAL or line 242 with NTSC. The display control unit selects one of the stored eight pages for display. The 8-bit character words are transformed into a 6 x 10 dot matrix with PAL or 6 × 8 dot matrix with NTSC by a character generator (ROM) of 96 programmed characters and are displayed in 24 rows of 40 characters each. Different character sets are available for eight languages under CCU or transmitter control, the required character set being selected automatically by the control bits C_{12} to C_{14} of row 0 of the Teletext page displayed. Every tenth line with PAL or every eighth line with NTSC a new Teletext row is loaded from the RAM into the RAM buffer. When the RAM is not accessed by the TPU 2732, the memory control refreshes the memory and handles CCU requests for RAM access.

Via the IM bus the CCU can read from and write into all RAM locations and controls the TPU 2732 by loading the appropriate registers in the RAM, so that the TPU 2732 can be used to display text from other sources. The TPU 2732 can display a list of contents of the stored eight pages (menu) all by itself.

As external RAM can be used either one 64 K x 1 bit Dynamic RAM or one 16 K x 1 bit Dynamic RAM. So, the RAM capacity is flexible to store 2 or 8 pages. The RAMs can be standard types (see section 3.).

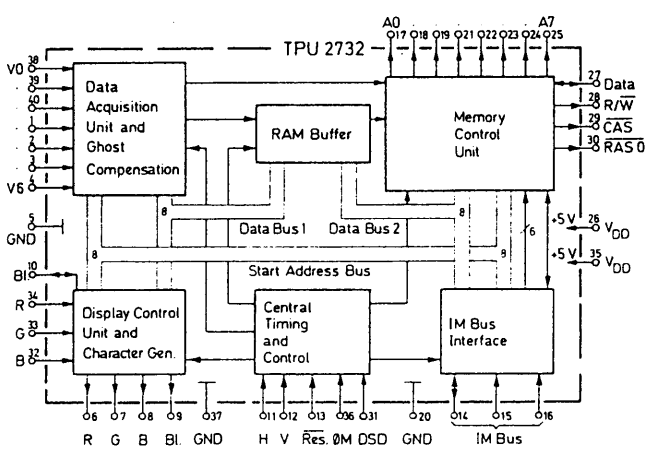


Fig. 2: Block diagram of the TPU 2732

MCU 2600
Clock Generator IC

Clock Generator IC

Integrated circuit in CI technology for generating the main clock ∅M for digital TV receivers according to the DIGIT 2000 concept.

1. Introduction

The MCU 2600 Clock Generator IC supplies the digital signal processors, decoders, converters etc. of the DIGIT 2000 digital TV system with the required main clock signal, which is of trapezoidal shape, with rounded corners, in order to avoid interference. For PAL and SECAM, the clock frequency is four times the PAL color subcarrier frequency, and for NTSC, the clock frequency is four times the NTSC color subcarrier frequency:

for PAL and SECAM: $f_{\varnothing M} = 4 \times 4.433\,618\,75\ \text{MHz} = 17.734\,475\ \text{MHz}$

for NTSC: $f_{\varnothing M} = 4 \times 3.579\,545\ \text{MHz} = 14.318\,180\ \text{MHz}$

for D2-MAC: $f_{\varnothing M} = 20.25\ \text{MHz}$

2. Functional Description

As can be seen from the block diagram Fig. 2-1, three VCOs (voltage-controlled oscillators) integrated in the MCU 2600 Clock Generator IC (one for PAL and SECAM, one for NTSC, and one for D2-MAC operation) form part of a PLL (phase-locked loop) circuit, the other parts of which, the phase comparator and the digital PLL filter are placed in the VPU 2203 or the CVPU 2233 or the CVPU 2235 or the DMA 2270. The filtered phase difference signal $\Delta\varphi$ is supplied in digital serial form (Fig. 2-2) to pin 6 of the MCU 2600. This data transfer is controlled by means of the data clock signal which is fed to pin 5 of the MCU 2600 and whose frequency is ¼ of the main clock signal ∅M.

With the negative transition of the data clock signal, the data is written into the shift register, and with the positive transition, the content of the shift register is shifted by 1 bit. After 12 bit have been written into the shift register and the data clock signal has attained again the stable high level (Fig. 2-2), an internal delay of about one data clock period occurs. This following, the data are taken over into the parallel register. From there, the information is fed to the oscillator control circuit and to the 9-stage D/A converter that produces the tuning voltage for the three voltage-controlled oscillators. The write-and-store cycle is initiated at the begin of each horizontal sweep.

The closed control loop ensures a phase-true locking between the oscillator signal (from which is produced the ∅M main clock) and the color subcarrier burst or the digital data burst contained in the received signal.

The signal produced by the VCO in action, is transferred to the filter via the oscillator control circuit. The filter forms the required main clock ∅M and is followed by the output buffer that provides a low-impedance output signal suited for clocking the DIGIT 2000 signal processors.

The timing of the data transfer from the VPU 2203, CVPU 2233 or CVPU 2235 Video Processor or the DMA 2270 D2-MAC Decoder to the MCU 2600 Clock Generator IC is illustrated in Fig. 2-2. The first three bits serve for selecting the required VCO, depending on whether PAL/SECAM, NTSC, or D2-MAC operation is chosen. The following nine bits (LSB first) provide the tuning signal for the VCO in the shape of two's complement. These nine bits are composed of the filtered sign-containing phase deviation $\Delta\varphi$ (7 bits) and the sign-containing alignment value for the oscillator (8 bits).

If the MCU 2600 Clock Generator IC is employed in a multi-standard TV set, the required VCO is selected in the way already described. For use in a single-standard receiver, the selection of the operating VCO is free and independent of the data signal. The not-used oscillators can be blocked externally by applying ground to pins 9, 10 or 12. In the case of a multi-standard TV set with up to three operated VCOs, the priority level for operation is internally fixed with the highest level for VCO 1 and the lowest level for VCO 3. This means, when switching on and also in the case of data faults the oscillator control circuit will select the oscillator with the highest level, if the input of this oscillator is not externally grounded.

It should be noted that all connection rails on the PC board must be designed under the point of view of HF signals. An inductance of 10 nH/cm can be assumed at a 0.5 to 1 mm wide rail. This makes an inductive impedance of several Ohms per cm length for the important 3rd harmonic of $f_{\varnothing M}$. Best performance is given by ground plaine layout of the PC board. All ground and signal lines should be as wide as possible, inductance-free and without loops in the neighbourhood of high HF currents. All supply pins of the clock generator IC must be equipped with ceramic bypass capacitors directly at the IC to ground pins on the shortest possible way.

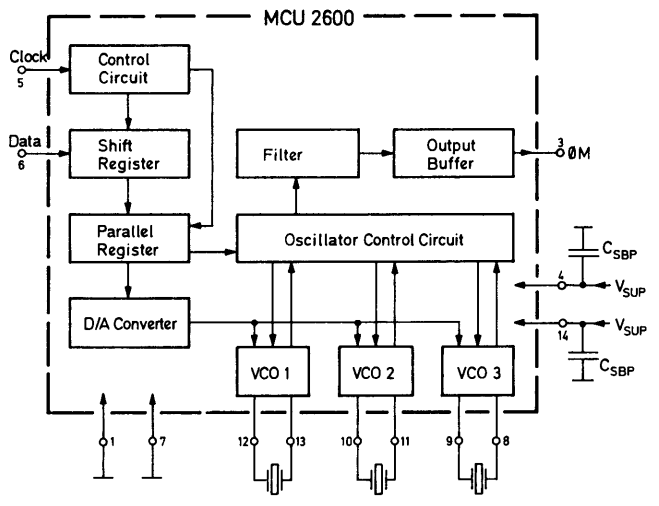


Fig. 2-1: Block diagram of the MCU 2600 clock generator and application circuit

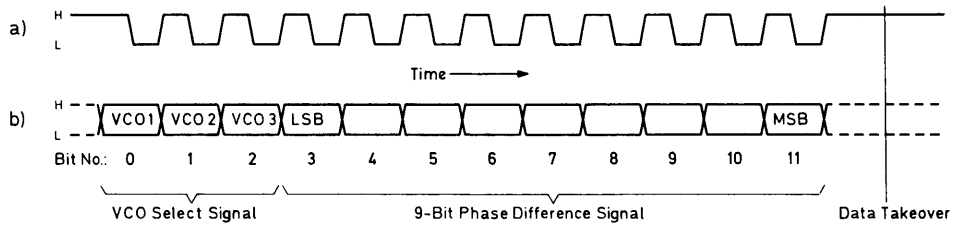


Fig. 2-2:
Timing of the data transfer from CCU via the VPU, CVPU or DMA to the MCU 2600
a) PLL clock fed to pin 5,
b) PLL data fed to pin 6,

3. Outline Dimensions and Pin Connections

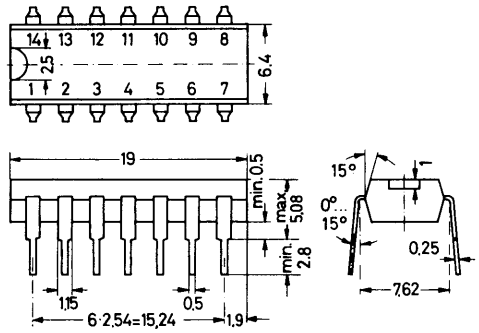


Fig. 3-1:
MCU 2600 in 14-pin Dil Plastic Package,
20 A 14 according to DIN 41 870

Weight approx. 1 g Dimensions in mm

Pin Connections

1	Ground of Output Buffer
2	leave vacant!
3	Main Clock Output ∅M
4	V_{SUP} Output Buffer Supply
5	PLL Clock Input
6	PLL Data Input
7	Ground
8	Output VCO 3 (D2-MAC)
9	Input VCO 3 (D2-MAC)
10	Input VCO 2 (NTSC)
11	Output VCO 2 (NTSC)
12	Input VCO 1 (PAL, SECAM)
13	Output VCO 1 (PAL, SECAM)
14	V_{SUP} Supply Voltage

4. Electrical Characteristics

All voltages are referred to ground.

4.1. Absolute Maximum Ratings

Symbol	Parameter	Pin No.	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–	0	65	°C
T_S	Storage Temperature	–	−40	+125	°C
V_{SUP}	Supply Voltage	4, 14	–	6	V
V_{VCOI}	VCO Input Voltage	9, 10, 12	–	6	V
V_{VCOO}	VCO Output Voltage	8, 11, 13	–	6	V
I_{PI}	PLL Bus Input Current	5, 6	–	2	mA
$I_{\varnothing MO}$	∅M Clock Output Current	3	−100	+100 x)	mA

x) It is not permitted to connect the output to ground continuously.

6. Description of the Connections and Signals

Pin 1 – Ground of Output Buffer
This pin serves as separate ground pin for the output buffer and must be carefully decoupled from the crystal oscillators and the input signals.

Pin 3 – ∅M Main Clock Output (Fig. 5-1)
This pin supplies the clock signal for the DIGIT 2000 TV receiver for clocking all signal processors used in this system.

Pin 4 – V_{SUP} Output Buffer Supply
A positive supply voltage of 5 V is required which powers the output buffer and must be well decoupled with respect to the other supply pin. For this, a bypass capacitor is required between pins 4 and 1.

Pin 5 – PLL Clock Input (Fig. 5-2)
Via this pin the MCU 2600 Clock Generator receives the PLL clock for transferring the tuning signal from the VPU, the CVPU or the DMA to the VCO integrated in the MCU 2600.

Pin 6 – PLL Data Input (Fig. 5-2)
The desired oscillator is selected by the signal fed to pin 6 as described in Table 4-1. Additionally, pin 6 receives the digital PLL information supplied by the VPU, the CVPU or the DMA, to control the VCO included in the MCU 2600 Clock Generator.

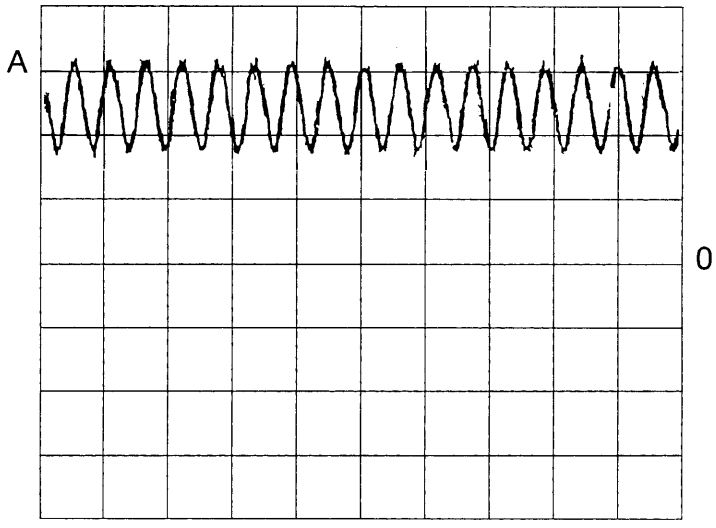
Pin 7 – Ground
This pin serves as ground pin for the whole circuit except the output buffer. Its connection should be separated carefully from the pin 1 ground connection.

Pins 8 to 13 – Crystal Connections (Fig. 5-3)
In addition to the oscillator function, the respective input pin serves also for switching off the not-used oscillators by connecting their input pins to ground (pin 7).

Pin 14 – V_{SUP} Supply Voltage
This pin is the supply pin for the whole IC except the output buffer. It must be decoupled carefully with respect to the output buffer supply pin 4. For this, a bypass capacitor between pins 14 and 7 is required.

MCU

PIN 3



TIMEBASE .1 µsec/div
AMPL. 1 V/cm DC

MDA 2062
1024-Bit EEPROM

1024-Bit EEPROM

Electrically erasable programmable read-only memory (EEPROM) in N-channel floating-gate technology with a capacity of 128 words, 8 bits each.

The MDA 2062 is intended for use as a reprogrammable non-volatile memory in conjunction with the CCU 2030/2050/2070 series Central Control Units of the DIGIT 2000 Digital TV System, the MAA 4000 Remote-Control and PLL-Tuning Microcomputers for TV receivers or the SAA 1280, SAA 1290 and SAA 1293 Remote-Control and Tuning ICs. It serves for storing the tuning information as well as several analog settings, further alignment information given in the factory when producing the TV set. The stored information remains stored even with the supply voltages switched off. Reading and programming operations are executed via the IM bus (see section 7.). Input and output signals are TTL level. An address option input provides the possibility to operate two memories in parallel, to obtain a total storage capacity of 2048 bits.

1. Functional Description

1.1. Memory Operation

The internal memory address space ranges from address 128 to address 255. Addresses 4 and 14 provide special functions.

To read a stored data word, the desired memory address has to be entered to the memory address register first. This is done by serially entering the IM bus address 128 (optionally 132) (during Ident = L), followed by the memory address (during Ident = H) in a single IM bus operation.

With the memory address register set, the memory data may be read. This, in turn, is done by entering the IM bus address 129 (optionally 133) to the device (during Ident = L). Immediately after this, within the same IM bus operation (during Ident = H) the open-drain Data output will conduct to serially transmit the respective 8-bit memory data.

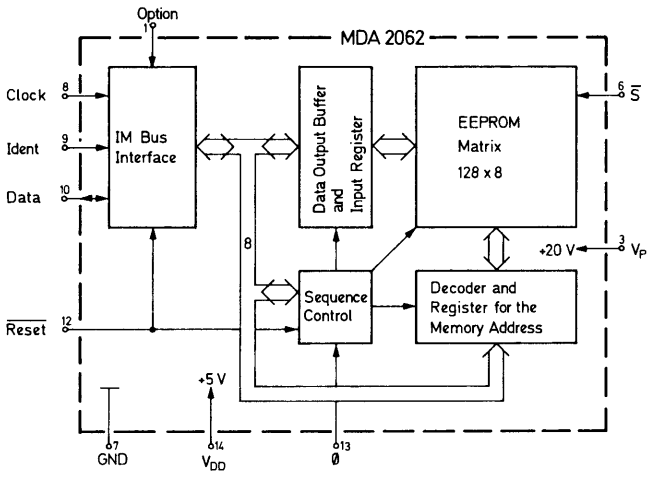


Fig. 1: Block diagram of the MDA 2062 EEPROM

Reprogramming a memory location is done in two steps, a) and b), that are identical except for the data word to be entered. Step a) resets all bits to "1", and step b) programs the desired data into the selected memory location.

a) First, the desired memory address is entered in the way described above. Second, the actual programming is initiated by serially entering the IM bus address 131 (optionally 135) followed by the data word to be stored, which is 255 for step a). The device will now internally time its programming sequence of approx. 16 periods of the 1 kHz memory clock. During this "busy" time all inputs are blocked from affecting the programming except for the $\overline{\text{Reset}}$ input. A $\overline{\text{Reset}}$ = L signal will immediately cancel any programming operation as well as any bus operation in progress.

The busy state may be interrogated by reading bit 1 of address location 14. A high level of this "busy-bit" indicates that programming is still under way. The IM bus operation for entering address 14 should always directly precede reading the busy-bit.

Reading any other address location during the busy state will produce erroneous data at the Data output. An address change operation during the busy state will not change the memory address register content. The intended start of another programming operation during the busy time will not be executed.

b) After time-out, normal operation may be resumed, e. g. by performing the second step of a programming sequence, i. e. by programming the desired 8-bit data word into the respective memory address location. This is done by restoring the proper memory address first, if necessary, and then by serially entering the IM bus address 131 (optionally 135) followed by the desired 8-bit data word. The device will again time its own programming sequence as described under a). After time-out the new data may be verified.

1.2. Redundancy

The MDA 2062 EEPROM contains circuitry that allows to replace up to two rows of the memory matrix, each containing 4 bytes of memory, by redundant rows SR 1 and SR 2. This substitution can be done in the field, by the user.

To prepare for activation of SR 1, memory address location 192 must contain the 5 LSB of the memory address containing the defect, which identifies the row to be substituted. Furthermore, bit 5 has to be set to "0", which identifies the data to be redundancy relevant (see Fig. 2).

To prepare for activation of SR 2, memory address location 160 must contain the equivalent data.

7	6	5	4	3	2	1	0
X	X	$\overline{\text{SR1 enable}}$	5 LSB of Defect Memory Address ≙ Address of Row to be Substituted				
			A4	A3	A2	A1	A0

Fig. 2: Activation of redundant row SR 1

The activation itself of the redundant rows is done by reading the content of memory address locations 192 and 160. This transfers the repair information stored nonvolatilely in the memory array to volatile repair registers.

It is important to note that the repair registers are cleared (bit 5 set to "1") by any $\overline{\text{Reset}}$ = L signal. Thus, any LH transition of the $\overline{\text{Reset}}$ signal must immediately be followed by reading the memory address locations 192 and 160, which restores the repair information to the repair registers.

SR 2 may be substituted by SR 1, whereas SR 1 cannot be substituted. As well, row 0 which contains the memory address locations 192 and 160 cannot be substituted.

SR 1 and SR 2 are part of the memory matrix portion that is not protectable by the $\overline{S}$ signal. Memory address locations 192 and 160 are part of the protectable portion.

1.3. Testing

The MDA 2062 EEPROM contains circuitry designed to facilitate testing of the various functions. By programming data into address location 4, the device is switched to one or more of a number of test modes. A detailed description is given in section 6.

1.4. Protected Matrix

The programming matrix contains a protectable portion. Addresses 128 to 134, 160 to 166, 192 to 198 and 224 to 230 can only be programmed if the "Safe" input $\overline{S}$ (pin 6) is at high potential. In that way, this portion of the memory is protected against inadvertent reprogramming even if such false informations were received via the IM bus. The second part of the programming matrix is not protected.

1.5. Shipment

Parts are shipped with all bits set to "1", except for addresses 192 and 160 which may contain repair information. The content of memory address locations 192 and 160, if different from 255, should not be altered, as this will result in defective rows appearing within the memory address space.

2. Outline Dimensions and Pin Connections

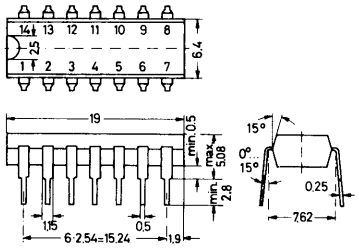


Fig. 3:
MDA 2062 in 14-pin Dil Plastic Package TO-116, 20 A 14 according to DIN 41870

Weight approx. 1.2 g Dimensions in mm

Pin Conncetions

1	Option Input
2	NC
3	Programming Voltage V_P
4	NC
5	NC
6	Safe Input $\overline{S}$
7	Ground, 0
8	IM Bus Clock Input
9	IM Bus Ident Input
10	IM Bus Data Input/Output
11	NC
12	$\overline{\text{Reset}}$ Input
13	Memory Clock Input
14	Supply Voltage V_{DD}

5. Description of the Connections and the Signals

Pin 1 – Option Input
Fig. 5 shows the internal configuration of this input. With Pin 1 at ground potential (low) or floating, the MDA 2062 reacts upon the IM bus addresses 128, 129 and 131. With pin 1 continuously at V_{DD} potential (high), the MDA 2062 reacts upon this IM bus addresses 132, 133 and 135 (see Fig. 8). In this way, parallel operation of two MDA 2062 is permitted, to obtain 2048 bits of non-volatile storage directly accessible via the IM bus. Pin 1 is internally tied to ground via a transistor equivalent to a 40 kΩ resistor.

Pins 2, 4, 5 and 11 – NC
These pins are not connected internally.

Pin 3 – Programming Voltage V_P
A programming voltage of + 20 V (± 5 %) is required. The current consumption during programming is approximately 1 mA. During non-programming operations, pin 3 may be held at any level between (V_{DD} – 0.7 V) and + 21 V. It may also be left floating. The MDA 2062 EEPROM **must not** be inserted or removed from a socket with $V_P \geq 6$ V. During power on/off sequences, current from the V_P supply should be limited to $I_{P\,max} = 5$ mA.

Pin 6 – Safe Input $\overline{S}$
Fig. 5 shows the internal configuration of this input. Normally, with pin 6 at ground potential (low), one portion of the programming matrix is protected so that this part of the memory cannot be reprogrammed inadvertently. Only when pin 6 receives high potential continuously, the protected portion of the memory matrix can be programmed. Pin 6 is internally tied to ground via a transistor equivalent to a 40 kΩ resistor.

Pin 7 – Ground, 0
This pin must be connected to the negative of the supplies.

Pins 8 to 10 – IM Bus Connections
These pins serve to connect the MDA 2062 EEPROM to the IM bus (see section 7.), via which it communicates with the CCU 2030/2050/2070 or MAA 4030 series µC or the SAA 1280/SAA 1290/SAA 1293. Pins 8 (IM Bus Clock Input) and 9 (IM Bus Ident Input) are inputs as shown in Fig. 6 and pin 10 (IM Bus Data) is an input/output as shown in Fig. 7. The signal diagram for the IM bus is illustrated in Figs. 8 and 11. The required addresses which the MDA 2062 EEPROM receives from the microcomputer, are also shown in Fig. 8.

Pin 12 – $\overline{\text{Reset}}$ Input
This input has a configuration as shown in Fig. 6. Via this input, the MDA 2062, together with the other circuits belonging to the system, receives the $\overline{\text{Reset}}$ signal which is derived from V_{DD} via an external RC circuit. A low level is required during power-up and power-down procedures. Low level at pin 12 (max. 1.3 V) cancels a programming procedure and an IM bus operation in progress. The memory address register is not, the repair register is erased. During operation, pin 12 requires high level (min. 2.4 V).

Pin 13 – Memory Clock Input
Via this input (Fig. 6) the MDA 2062 receives a 1 kHz clock signal from pin 3 of the CCU 2030, CCU 2050, CCU 2070 or MAA 4030 microcomputer or the SAA 1280/SAA 1290/SAA 1293.

Pin 14 – Supply Voltage V_{DD}
The supply voltage required is + 5 V (± 5 %), and the current consumption in active operation is approx. 30 mA.

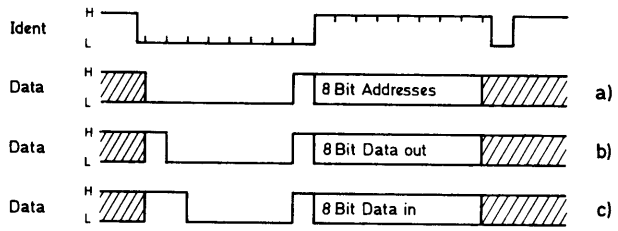


Fig. 8: Signal diagram for the IM bus

	Pin 1 low	Pin 1 high	
a) enter memory address:	128	132	followed by address
b) reading:	129	133	followed by data out
c) programming:	131	135	followed by data in

6. Test Functions

This description of the test byte is not part of the specification. It contains no information necessary for normal (intended) use of the MDA 2062 memory. It is only intended as a description of the various functions of the test byte that are designed for factory use, but it does not specify such properties. The description is subject to change.

Address location 4 contains a test byte which governs test mode operation of the MDA 2062. The test byte is set by performing the IM bus operation for entering address 4, followed by an IM bus programming operation with the desired test data word. The test byte is valid during all following IM bus operations until changed or set to 0 by a $\overline{\text{Reset}}$ = L signal. The test byte shall not be changed during the busy time of a programming operation. Fig. 9 shows the bit arrangement of the test byte. Set bit 5 for activation of the test byte!

Block Programming
Three block program modes can be activated by the test byte, in conjunction with the memory address loaded into the memory address register:

	memory address 7 6 5 4 3 2 1 0	
1) all bytes are selected (including 8 bytes in redundant rows):	1 x x x x x 0 x	(e. g. 128)
2) all even-numbered bytes are selected (redundant bytes are not predetermined, they have to be defined as even bytes):	1 x x x x x 1 0	(e. g. 130)
3) all odd-numbered bytes are selected (redundant bytes are not predetermined):	1 x x x x x 1 1	(e. g. 131)

7	6	5	4	3	2	1	0
Block programming enable	Read reference shift −0.3 V	Test Byte enable	Read reference shift −0.6 V	Ramp disable	Read reference shift +0.3 V	Redundancy disable	Read reference shift +0.6 V

Fig. 9: Functions of the 8 bits in the test byte

Thus, programming all selected bytes with the same desired data is done within one programming sequence. The complete sequence is:

Enter Address 4
Program Test byte (e. g. 160)
Enter Address 128, 130 or 131
Program Data

A checkerboard pattern is programmed with two programming operations after loading the test byte:

Enter Address 130
Program Data 85
Enter Address 131
Program Data 170

Read Reference Shifting
During read operations the memory cell threshold voltage is compared with a reference voltage. The comparator output then produces the logic one level for a cell threshold higher than the reference and the logic zero level for a cell threshold lower than the reference.

The test byte provides means to shift the reference voltage in positive or negative direction in three steps: ±0.3 V, ± 0.6 V and ± 0.9 V.

During a read operation a positive-shifted reference voltage establishes a margin test for logic ones, whereas a negative-shifted reference does so for logic zeroes. This margin test is performed digitally by IM bus operations only, without the need to switch analog power supplies.

	7 6 5 4 3 2 1 0
+ 0.9 V:	x 0 1 0 x 1 x 1
+ 0.6 V:	x 0 1 0 x 0 x 1
+ 0.3 V:	x 0 1 0 x 1 x 0
− 0.3 V:	x 1 1 0 x 0 x 0
− 0.6 V:	x 0 1 1 x 0 x 0
− 0.9 V:	x 1 1 1 x 0 x 0

Redundancy Disable
With bit one of the test byte set, the redundant rows can be accessed neither during byte program operations nor during any read operation, even if the redundancy registers are properly loaded. This test byte function has no effect on block programming operations.

Ramp Disable
The MDA 2062 contains circuitry to shape the internal program supply voltage to be a ramp function during programming operations. This feature is considered to be essential to a high erase/write endurance of the memory cells.

Bit 3 of the test byte disables this ramp function so that the internal program supply, according to the timing diagram Fig. 10, is immediately disconnected from the V_{DD} supply and connected to the V_P supply at the 4th falling edge of the 1 kHz memory clock, and is immediately disconnected from the V_P supply and re-connected to the V_{DD} supply at the 14th falling edge of the 1 kHz clock after the last rising Ident signal edge of the IM bus operation starting the program cycle. By this feature other than the built-in ramp function (approx. 100 µs/V) can be applied via the V_P supply pin.

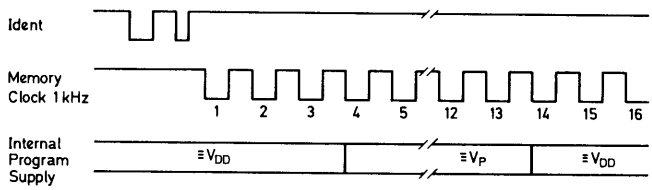


Fig. 10: Ramp disable timing diagram

7. Description of the IM Bus

The INTERMETALL Bus (IM Bus for short) has been designed to control the DIGIT 2000 ICs by the CCU Central Control Unit. Via this bus the CCU can write data to the ICs or read data from them. This means the CCU acts as a master whereas all controlled ICs are slaves.

The IM Bus consists of three lines for the signals Ident (ID), Clock (CL) and Data (D). The clock frequency range is 50 Hz to 170 kHz. Ident and clock are unidirectional from the CCU to the slave ICs, Data is bidirectional. Bidirectionality is achieved by using open-drain outputs with On-resistances of 150 Ω maximum. The 2.5 kΩ pull-up resistor common to all outputs is incorporated in the CCU.

The timing of a complete IM Bus transaction is shown in Fig. 11 and Table 1. In the non-operative state the signals of all three bus lines are High. To start a transaction the CCU sets the ID signal to Low level, indicating an address transmission, and sets the CL signal to Low level as well to switch the first bit on the Data line. Thereafter eight ad-

dress bits are transmitted beginning with the LSB. Data takeover in the slave ICs occurs at the High levels of the clock signal. At the end of the address byte the ID signal goes High, initiating the address comparison in the slave circuits. In the addressed slave the IM bus interface switches over to Data read or write, because these functions are correlated to the address.

Also controlled by the address the CCU now transmits eight or sixteen clock pulses, and accordingly one or two bytes of data are written into the addressed IC or read out from it, beginning with the LSB.

The Low clock level after the last clock pulse switches the Data line to High level. After this the completion of the bus transaction is signalled by a short Low state pulse of the ID signal. This initiates the storing of the transferred data.

It is permissible to interrupt a bus transaction for up to 10 ms.

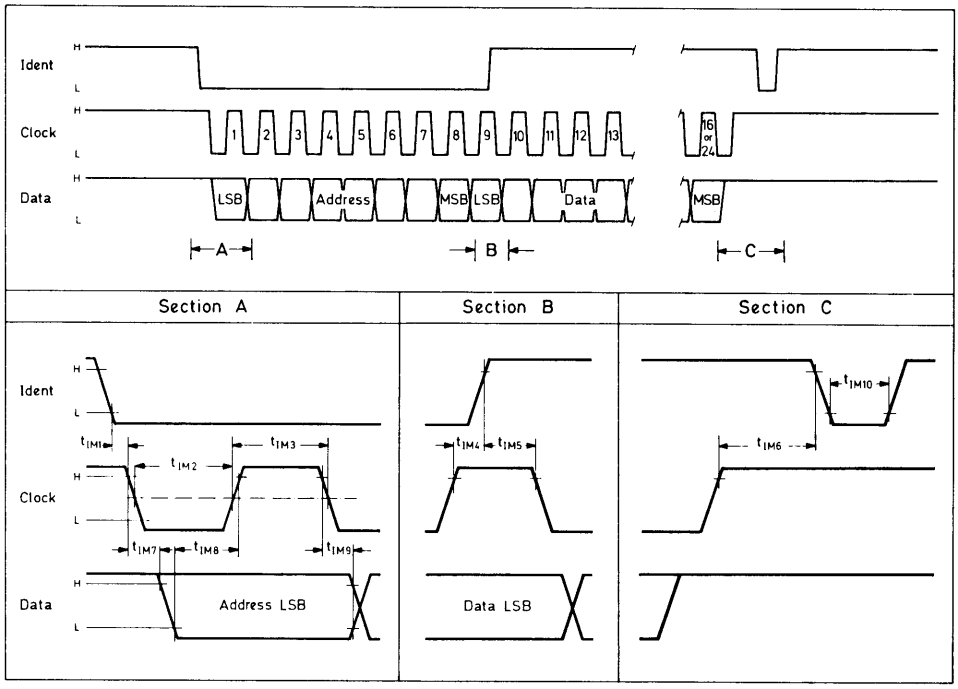


Fig. 11: Waveforms of the IM bus signals

Table 1: Timing of the IM bus signals

Time	t_{IM1}	t_{IM2}	t_{IM3}	t_{IM4}	t_{IM5}	t_{IM6}	t_{IM7}	t_{IM8}	t_{IM9}	t_{IM10}
Min. µs	0	3.0	3.0	0	1.5	6.0	0	0	0	3.0

ADC 2310 E
Audio A/D Converter

Audio A/D Converter

1. Introduction

Analog-to-digital converter for digitizing the analog stereo sound signals in digital TV receivers based on the DIGIT 2000 system, intended for working together with the APU 2400 T or the APU 2470 Audio Processor, being controlled by the CCU 2030, CCU 2050 or CCU 2070 Central Control Unit and being clocked by the MCU 2632 Clock Generator.

The ADC 2310 E is an integrated circuit in CI technology, housed in a 24-pin Dil plastic package, and contains on one silicon chip the following functions (see Fig. 1-1):

- several analog input and output amplifiers
- five analog switches (S1 to S5) for selecting different signal sources
- an analog stereo dematrix circuit
- a level control facility
- two pulse-density modulators (PDM I and PDM II)
- an IM bus interface

2. Functional Description

Fig. 2-1 shows the block diagram of a digital stereo sound channel intended for a DIGIT 2000 TV receiver, equipped with additional audio inputs and outputs which can be used with the so-called Euro connector or SCART connector, e. g. for connecting a video recorder.

The analog sound signals selected for conversion by the analog switch S1 firstly pass through the level control section where the desired level control is carried out. Thereafter, they are fed to the first processing stage of the A/D conversion, the pulse-density modulators PDM I and PDM II, whose output signals are 1-bit data streams with a data rate of 4.7 MHz maximum. This data is then transferred to the APU Audio Processor where the digital decimation filters are the input, performing the second step of the conversion process. Due to the very high sampling rate of the pulse-density modulators, no steep anti-aliasing filters are needed at the input. The digital output data of the whole converting system has a signal-to-noise ratio which can be compared to that of a conventional 13-bit A/D converter.

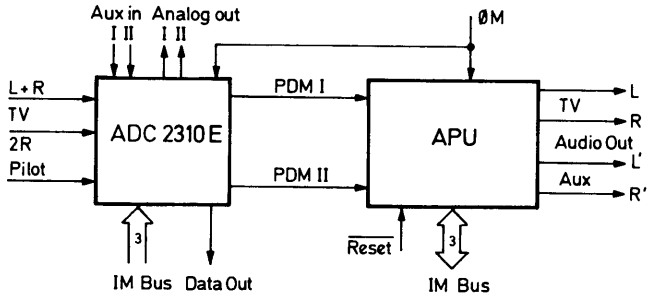


Fig. 2-1: Block diagram of a stereo sound channel composed of the ADC 2310 E Audio A/D Converter and the APU Audio Processor

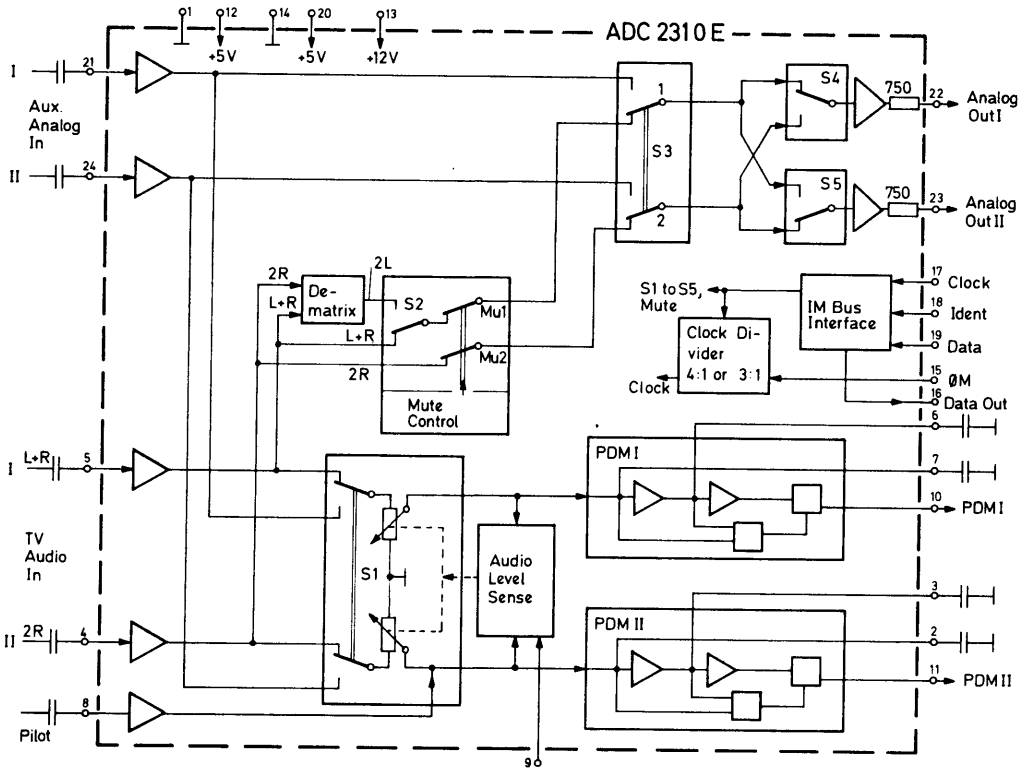


Fig. 1-1: Block diagram of the ADC 2310 E Audio A/D Converter

Table 2-1: Characteristics of the German TV stereo sound system

	Channel I	Channel II
Carrier Frequency for sound	Image Carrier – 5.5 MHz	Image Carrier – 5.742 1875 MHz
Sound Signal Mono Stereo Bilingual	 Mono L+R Language A	 Mono 2 R Language B
Identification Signals Carrier Frequency Modulation Modulation Depth	 – – –	 3.5 · f_H = 54.6875 kHz AM 50 %
Identification Frequencies Mono Stereo Bilingual	 – – –	 unmodulated f_H: 133 ≈ 117.5 Hz f_H: 57 ≈ 274.1 Hz

The TV Audio inputs get their analog signal (L+R and 2 R) from the stereo decoder of the TV set, whereas the Aux. Analog inputs are intended to receive an audio signal from a video recorder or another external source, e. g. via the SCART connector. The Analog Out I and II pins supply the selected audio signal, e. g., to the SCART connector for connection to a video recorder or other equipment.

2.1. The Analog Switches

The five analog switches S1 to S5 (S1 and S3 are two-pole switches) are controlled via the IM bus (see section 2.6.) to select the required connections between the four analog inputs and the two digital outputs and the two additional analog outputs.

2.2. The Dematrix

When switched on via the IM bus (switch 2, see Table 2-2), the dematrix provides the 2 R and 2 L stereo signals at the analog outputs. These signals are extracted form the L+R and 2 R input signals according to the German TV stereo sound system (see Table 2-1).

2.3. The Pulse-Density Modulators

The two pulse-density modulators, PDM I and PDM II, are sigma-delta modulators equipped with two feedback loops each. At the outputs they supply pulse trains whose pulse density is proportional to the amplitude of the input signal. The maximum sampling rate, and thus the maximum pulse rate, is 4.7 MHz.

2.4. The Level Control Section

This part of the ADC 2310 E serves to reduce the level of the input signal to be converted if the input signal exceeds the level for full drive of the PDM pulse-density modulators. Controlled by the IM bus, the audio level is sensed either in channel I or in channel II or in both channels. If all three possibilities are switched off, the capacitor at pin 9 is discharged rapidly to 2.8 V, and the level control goes to full level. The level control is under IM Bus control as shown in Table 2-2.

2.5. The Clock Divider

This part of the ADC 2310 E is provided for adapting the digital stereo sound channel to different TV standards. With bit 7 = Low (see Table 2-2), the divider ratio is set to 4:1, whereas bit 7 = High gives 3:1. This allows operation of the ADC 2310 E with almost the same sampling frequency at a main clock frequency ØM of 17.7 MHz (PAL) or 14.3 MHz (NTSC), both supplied by the MCU 2632 Clock Generator.

2.6. The IM Bus Interface

This circuit section is provided for controlling the ADC 2310 E by the CCU 2030, CCU 2050 or CCU 2070 Central Control Unit via the IM bus (see section 7.). In the case of ADC 2310 E, the IM bus is unidirectional from the CCU to the ADC. That means that information is only transferred from the CCU to the ADC 2310 E. The bit arrangement is shown in Fig. 2-2, and the actions performed can be derived from Table 2-2.

2.7. The Preemphasis and Deemphasis

The audio signal supplied by the stereo decoder or video demodulator of the TV set has a preemphasis determined

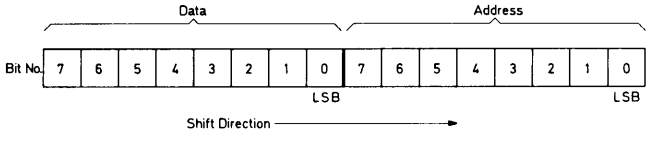


Fig. 2-2:
Shape of the data word given from the CCU to the ADC

Table 2-2: Addresses and commands sent from the CCU to the ADC 2310 E

Address Decimal	Bit No.	High Bit gives:	Low Bit gives:
96	0 (LSB)	Switch 5 on	Switch 5 off
96	1	Switch 4 on	Switch 4 off
96	2	Switch 3 on	Switch 3 off
96	3	Mute on	Mute off
96	4	Switch 2 on	Switch 2 off
96	5	Switch 1 on	Switch 1 off
96	6	Pin 16 High	Pin 16 Low
96	7 (MSB)	Clock Divider 3 : 1	Clock Divider 4 : 1
101	0 (LSB)	not used	
101	1	not used	
101	2	not used	
101	3	not used	
101	4	not used	
101	5	Channel I sensed	} Bits 5 + 6 Low give full
101	6	Channel II sensed	} gain in both channels
101	7 (MSB)	not used	

Unused bits should be set to Low.

at the transmitter. In a digital sound channel according to the DIGIT 2000 system this preemphasis is compensated after the APU Audio Processor by means of the RC element also used for suppressing the clock signal. In order to achieve a correct frequency response with an analog input signal via pins 21 or 24, a preemphasis with a similar response to the deemphasis after the APU must first be applied to these signals. Further, the analog output signal at pins 22 and 23 will have either the preemphasis used at the TV transmitter or that produced by the preemphasis network in front of pins 21 and 24. To have a proper audio signal available at pins 22 and 23, deemphasis capacitors are required at these pins, the resistors being integrated in the ADC 2310 E (750 Ω).

The preemphasis network in front of pins 21 and 24 ist suggested to have a time constant of 50 µs and, with 1 kHz, an attenuation of 7. This matches the usual conditions for the SCART connector, from which pins 21 and 24 normally receive their input signal.

3. Outline Dimensions and Pin Connections

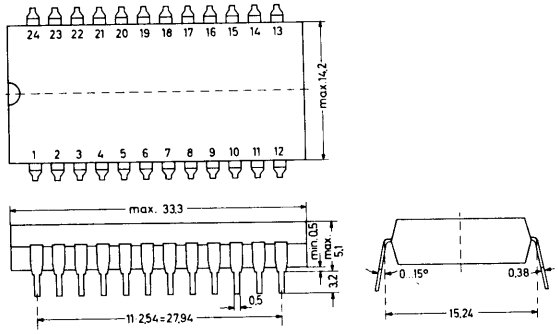


Fig. 3-1:
ADC 2310 E in 24-pin Dil Plastic Package
20 B 24 according to DIN 41 870

Weight approx. 4.5 g Dimensions in mm

Pin Connections

1	Ground (Analog)
2	Capacitor Pin
3	Capacitor Pin
4	Analog (TV) Audio Input II
5	Analog (TV) Audio Input I
6	Capacitor Pin
7	Capacitor Pin
8	Analog (TV) Pilot Input
9	Level Control RC Pin
10	PDM I Digital Sound Output
11	PDM II Digital Sound Output
12	V_{SUP1} Supply Voltage (An.)
13	V_{SUP2} Supply Voltage
14	Ground (Digital)
15	∅M Clock Input
16	Bit 6 Data Output
17	IM Bus Clock Input
18	IM Bus Ident Input
19	IM Bus Data Input
20	V_{SUP1} Supply Voltage (Digital)
21	Analog (Aux) Audio Input I
22	Analog Audio Output I
23	Analog Audio Output II
24	Analog (Aux) Audio Input II

4. Inner Configuration of the Connection Pins

The following figures schematically show the circuitry at the various pins.

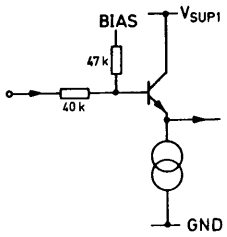


Fig. 4-1:
Input Pins 4 and 5

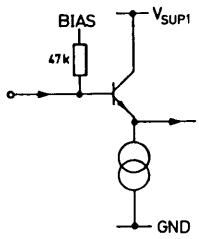


Fig. 4-2:
Input Pins 8, 21 and 24

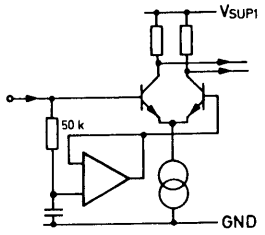


Fig. 4-3:
Input Pin 15

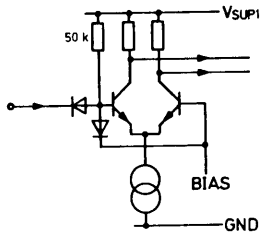


Fig. 4-4:
Input Pins 17 to 19

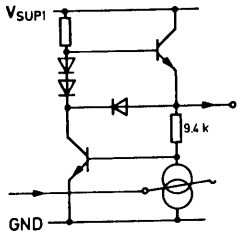


Fig. 4-5:
Output Pins 10 and 11

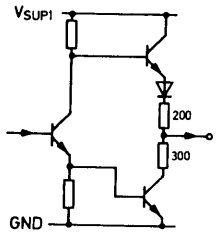


Fig. 4-6:
Output Pin 16

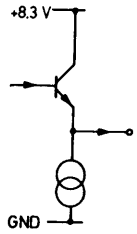


Fig. 4-7:
Output Pins 22 and 23

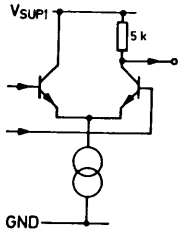


Fig. 4-8:
Capacitor Pins 2, 3, 6 and 7

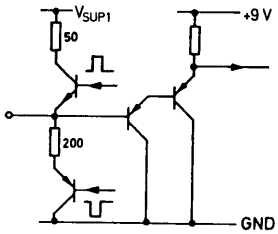


Fig. 4-9:
Level Control RC Pin 9

5. Discription of the Connections and Signals

Pin 1 – Ground (Analog)
This pin serves as ground connection for the analog input signals at pins 4, 5, 8, 21 and 24 and as ground connection for the supply of the analog part of the ADC 2310 E.

Pins 2, 3, 6 and 7 – Capacitor Pins (Fig. 4-8)
The filter capacitors for the inner and the outer feedback loop of the pulse-density modulators PDM I and PDM II must be connected to these pins.

Pins 4 and 5 – Analog (TV) Audio Inputs I and II (Fig. 4-1)
These two inputs get their input signal from the stereo decoder or sound demodulator of the TV set, coupled via capacitors. The input signal range can be increased by adding series resistors.

Pin 8 – Analog (TV) Pilot Input (Fig. 4-2)
It is possible to supply the ADC 2310 E with the pilot regardless of the position of switch S1 via this pin. The signal must be coupled capacitively.

Pin 9 – Level Control RC Pin (Fig. 4-9)
The RC element connected to this pin determines the response time of the level control circuit.

Pins 10 and 11 – PDM Digital Sound Outputs (Fig. 4-5)
These pins are the outputs of the pulse-density modulators PDM I and II which supply the PDM data to the APU Audio Processor.

Pin 12 – V_{SUP1} Supply Voltage (Analog)
The analog circuitry of the ADC 2310 E is supplied via this pin.

Pin 13 – V_{SUP2} Supply Voltage
The supply at this pin powers the analog switches.

Pin 14 – Ground (Digital)
This pin is the ground connection for the digital output signals supplied by pins 10 and 11 and for the supply of the digital part of the ADC 2310 E.

Pin 15 – ∅M Clock Input (Fig. 4-3)
This pin receives the required clock signal from the MCU 2632 Clock Generator.

Pin 16 – Bit 6 Data Output (Fig. 4-6)
This output provides the status of bit 6 (see Table 2-2).

Pins 17 to 19 – IM Bus Inputs (Fig. 4-4)
The ADC 2310 E is connected to the IM Bus and receives commands issued by the CCU via these pins.

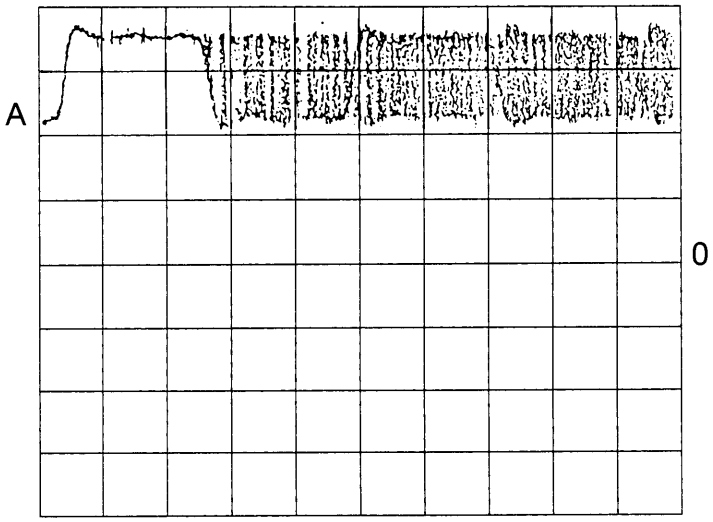
Pin 20 – V_{SUP1} Supply Voltage (Digital)
Pin 20 supplies the digital part of the ADC 2310 E.

Pins 21 and 24 – Analog (Aux) Audio Inputs I and II (Fig. 4-2)
These inputs can be used as playback inputs from a video recorder or other external sources, e. g. connected via the Euro or SCART connector. The input signal must be coupled via capacitors. The input signal range can be increased by adding series resistors.

Pins 22 and 23 – Analog Audio Outputs I and II (Fig. 4-7)
These two analog outputs provide either the signals of the TV inputs (pins 4 and 5) or the signals of the Aux inputs pins 21 and 24, depending on the state of the analog switches which are set by the CCU via the IM bus according to Table 2-2.

ADC

PIN 10/11



TIMEBASE .1 µsec/div
AMPL. 1 V/cm DC

APU 2470
Audio Processor

Audio Processor

1. Introduction

The APU 2470 Audio Processor is an N-channel MOS circuit, housed in a 24 pin Dil plastic package. It is designed to perform digital processing of TV audio information. The architecture of the APU 2470 combines two main blocks:

I/O blocks

DSP block

The I/O blocks are used to manage the input and output of audio information. The DSP block consists of a mask-programmable digital signal processor, whose software can be controlled by a microprocessor (CCU) via the IM bus. So parameters like coefficients can be modified during performance. By means of the DSP software, audio functions like dematrixing, bilingual mode, tone manipulation and volume control are performed. To allow bilingual performance two audio processing channels are available:

MAIN channel, provided for the loudspeaker system

AUX channel, provided for headphones

Fig. 1-1 gives an overview of the APU functions.

1.1. Application of the APU 2470

The APU2470 is designed to interface with ITT's ADC2310E Audio A/D Converter as well as with the DMA 2270 D2-MAC Decoder or the NIP 2400 NICAM Demodulator/Decoder and the AMU 2485 Audio Mixer. It can receive digital data in two different formats:

a) The ADC2310E receives analog audio information either from the SCART Interface, also called Euro connector (for example: video recorder) or from any terrestrial TV transmission and converts it into two 1-bit PDM streams. For this input format, decimation filters are provided in the APU2470, converting each PDM stream into a 16-bit word at a sampling rate of approximately 35 kHz.

b) Digital serial audio data, provided for example by the DMA 2270 D2-MAC Decoder or the NIP 2400 NICAM Demodulator/Decoder and mixed in the AMU 2485 Audio Mixer, can be received via the S bus by means of the S bus interface.

ITT's CCU 2030, CCU 2050, CCU 2070 or CCU 3000 Central Control Units of the DIGIT 2000 family are well suited for interfacing with the APU 2470 Audio Processor. Fig. 1-2 shows how the APU 2470 can be used together with the mentioned ITT ICs to realize multistandard audio processing with PAL and D2-MAC or NICAM signals. In the following descriptions data coming from the ADC will be called "PDM-Data", and data from the AMU will be called "S-Data".

Two different audio configurations are possible with the APU 2470 (Fig. 1-2). The dashed line version uses the AMU 2485 as a preprocessing unit both for PDM-Data and S-Data and allows mixing between both kinds of inputs. Another advantage of this version is the digital 50 µs deemphasis included in the AMU 2485 applied to the PDM inputs. This gives the flexibility to switch between the D2-MAC/NICAM J17 deemphasis and the FM 50 µs deemphasis without using analog means. This version is recommended for new TV concepts. The other application needs an analog 50 µs deemphasis in case of S-Data input in the AMU 2485. For that reason a switchable 50 µs preemphasis is included in the AMU 2485. This version can be used in conjunction with the old ADC-APU concept.

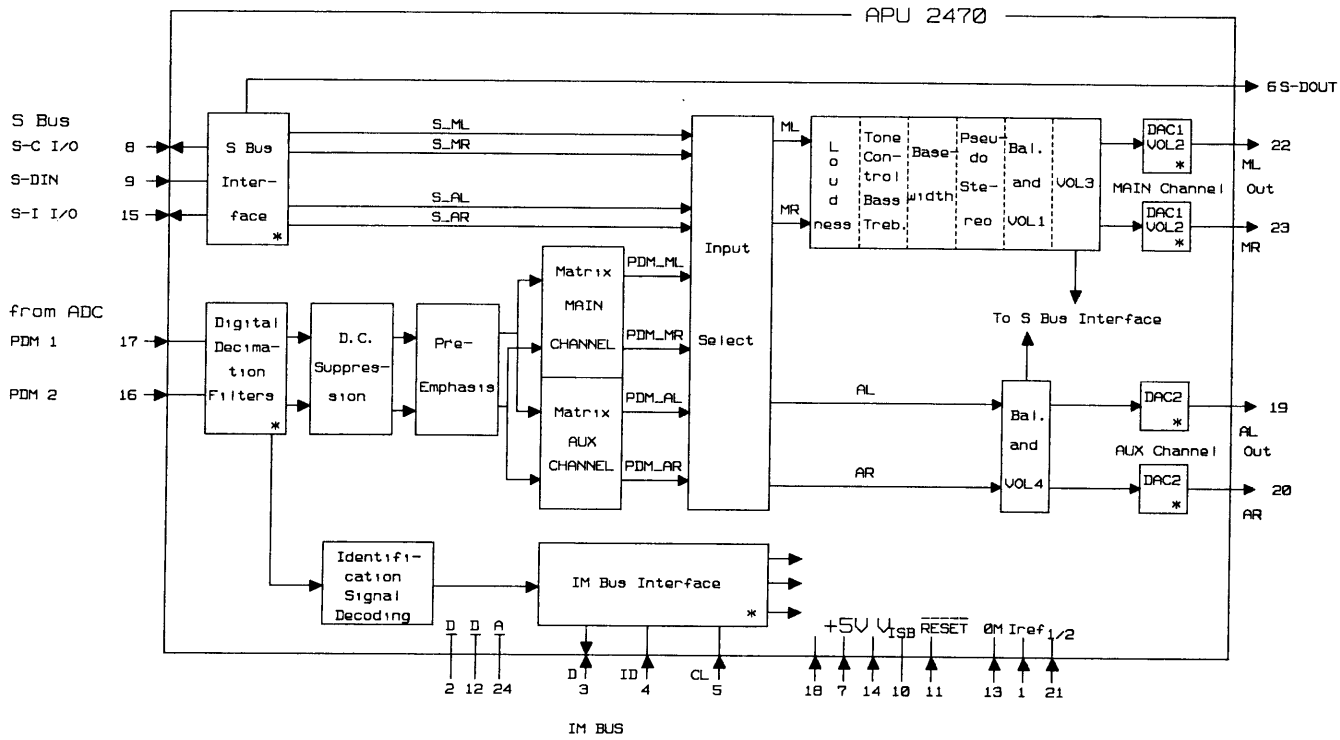


Fig. 1-1: Functional block diagram of the APU 2470. The hardware interfaces are marked by an asterisk*.

5. Specifications

5.1. Outline Dimensions

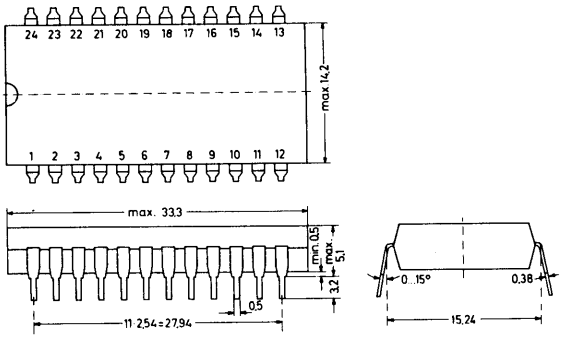


Fig. 5-1:
APU 2470 in 24-pin Dil Plastic Package,
20 B 24 according to DIN 41 870

Weight approx. 4.5 g Dimensions in mm

5.2. Pin Connections

1 $I_{REF\,2}$ Reference Current Input (for AUX DACs)
2 Ground (Digital)
3 IM Bus Data Input/Output
4 IM Bus Ident Input
5 IM Bus Clock Input
6 S-Data Output
7 V_{SUP} Supply Voltage (Digital)
8 S-Clock Input/Output
9 S-Data Input
10 V_{ISB} Internal Substrate Bias Voltage
11 $\overline{\text{Reset}}$ Input
12 Ground (Digital)
13 ∅M Clock Input
14 V_{SUP} Clock Buffer Supply Voltage (Digital)
15 S-Ident Input/Output
16 PDM II Digital Input (R)
17 PDM I Digital Input (L)
18 V_{SUP} Supply Voltage (Digital)
19 AUX DAC Output 2L
20 AUX DAC Output 2R
21 $I_{REF\,1}$ Reference Current Input (for MAIN DACs)
22 MAIN DAC Output 1L
23 MAIN DAC Output 1R
24 Ground (Analog)

5.3. Pin Descriptions

Pins 1 and 21 – Reference Current Inputs (Fig. 5-2)
These inputs require a current of 150 µA called reference current I_{REF} and serving for volume adjustment in the DAC interfaces.

Pins 2 and 12 – Digital Ground, 0
These pins must be connected to the negative of the supply. They have to be used for ground connections in conjunction with digital signals.

Pins 3, 4 and 5 – IM Bus Connections
Via these pins, the APU 2470 is connected to the IM bus and communicates with the CCU. Pins 4 (IM bus Ident input) and 5 (IM bus Clock input) have the configuration shown in Fig. 5-3. Pin 3 (IM bus Data input/output) is shown in Fig. 5-7. The IM bus is described in section 2.1.3.

Pins 6, 8, 9 and 15 – Serial Audio Interface (S Bus)
Pin 9 is the S-Data input (Fig. 5-6) and pin 6 the S-Data output (Fig. 5-9). Pins 8 and 15 are S-Clock and S-Ident inputs/outputs (Fig. 5-8), the status depending on bit 4 in coefficient k33 (see sections 2.1.2. and 4.13.).

Pins 7, 14 and 18 – V_{SUP} Supply Voltage
These pins must be connected to the positive of the supply. The clock buffer supply pin 14 must be decoupled carefully from the other supply pins.

Pin 10 – V_{ISB} Internal Substrate Bias Voltage
The APU 2470 has an on-chip substrate bias generator which produces a negative bias voltage of about 3.4 V. Pin 10 should have a 0.1 µF capacitor to ground.

Pin 11 – $\overline{\text{Reset}}$ Input (Fig. 5-3)
In the steady state, high level is required at pin 11. A low level normalizes the APU 2470. Initialization of the APU 2470 is described in section 4.12.

Pin 13 – ∅M Main Clock Input (Fig. 5-4)
This pin receives the required main clock signal from the MCU 2600 or MCU 2632 Clock Generator IC or from the DMA 2270 D2-MAC Decoder or the NIP 2400 NICAM Demodulator/Decoder.

Pins 16 and 17 – $\overline{\text{PDM II}}$ and $\overline{\text{PDM I}}$ Digital Inputs (Fig. 5-5)
These pins receive the pulse-density modulated output signals of the ADC 2300 E or ADC 2310 E.

Pins 19 and 20 – AUX DAC Outputs 2L and 2R (Fig. 5-9)
These pins supply the audio output signals as output currents whose amplitude is determined by the reference current $I_{REF\,2}$ fed to pin 1. The output signal of pins 19 and 20 is not influenced by the VOL 1 and VOL 2 volume controls and is intended for headphones, for example.

Pins 22 and 23 – MAIN DAC Outputs 1L and 1R (Fig. 5-9)
These pins supply the audio output signals as output currents whose amplitude is determined by the reference current $I_{REF\,1}$ fed to pin 21. The output signal of pins 22 and 23 is influenced by the VOL 1 and VOL 2 volume control facilities.

Pin 24 – Analog Ground 0
This pin must be connected to the negative of the supply. It serves as ground connection for analog signals.

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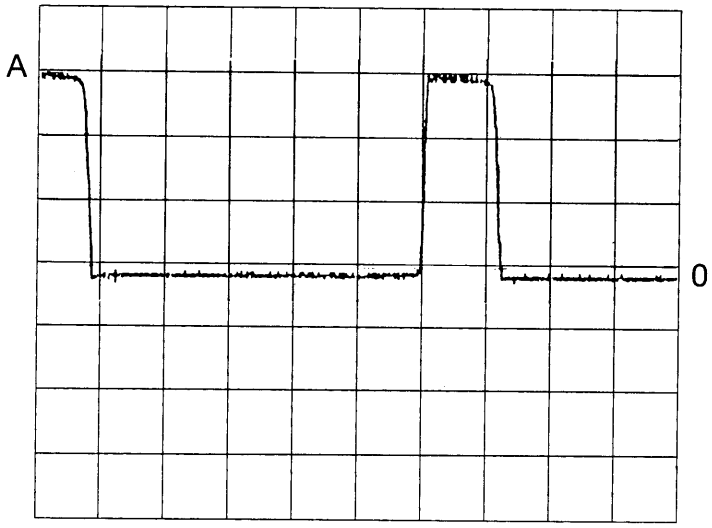
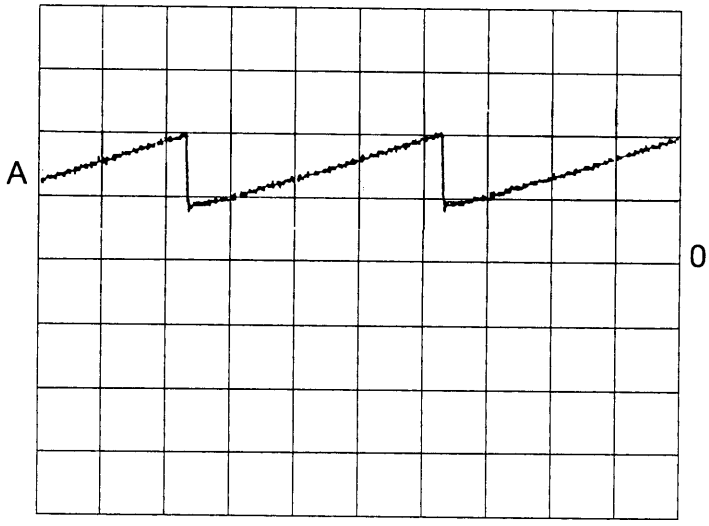
PIN 6



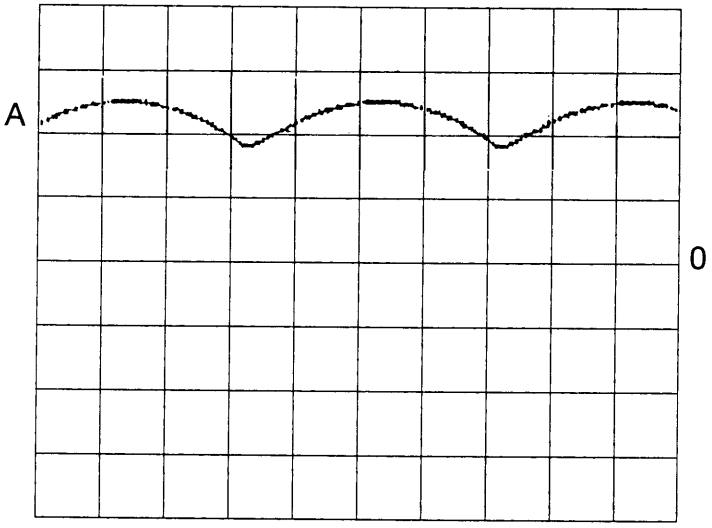
TIMEBASE 10 µsec/div
AMPL. 2 V/cm DC

PIN 7



TIMEBASE 5 msec/div
AMPL. 2 V/cm DC

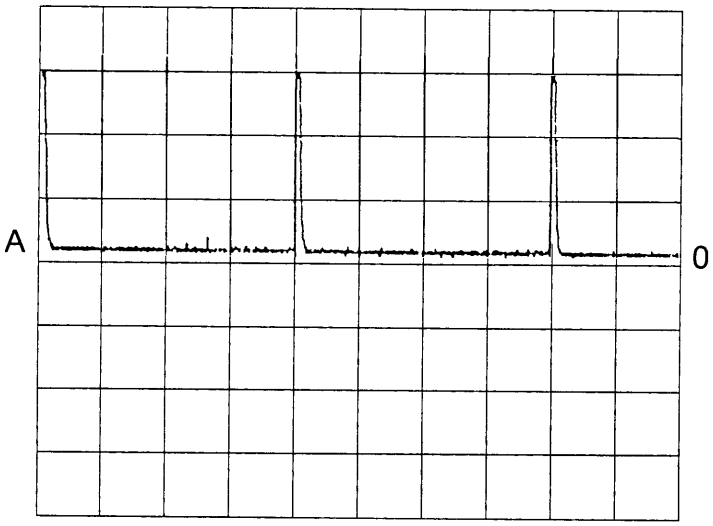
PIN 8



TIMEBASE 5 msec/div
AMPL. 2 V/cm DC

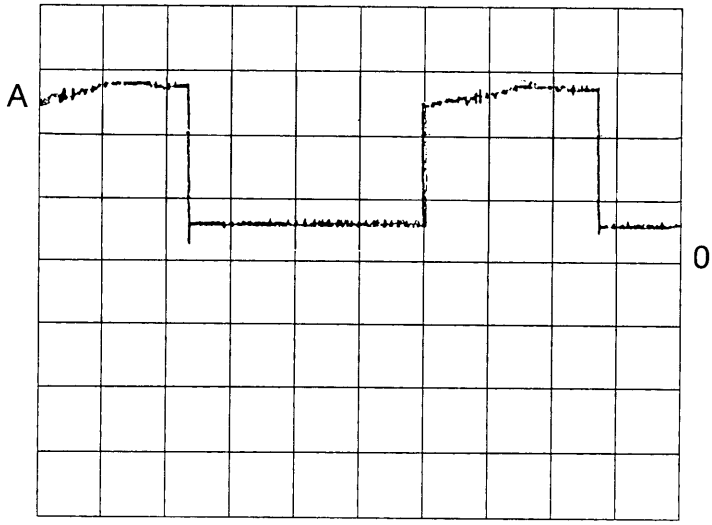
Stecker ST DT

PIN 9



TIMEBASE 5 msec/div
AMPL. 2 V/cm AC

PIN 11



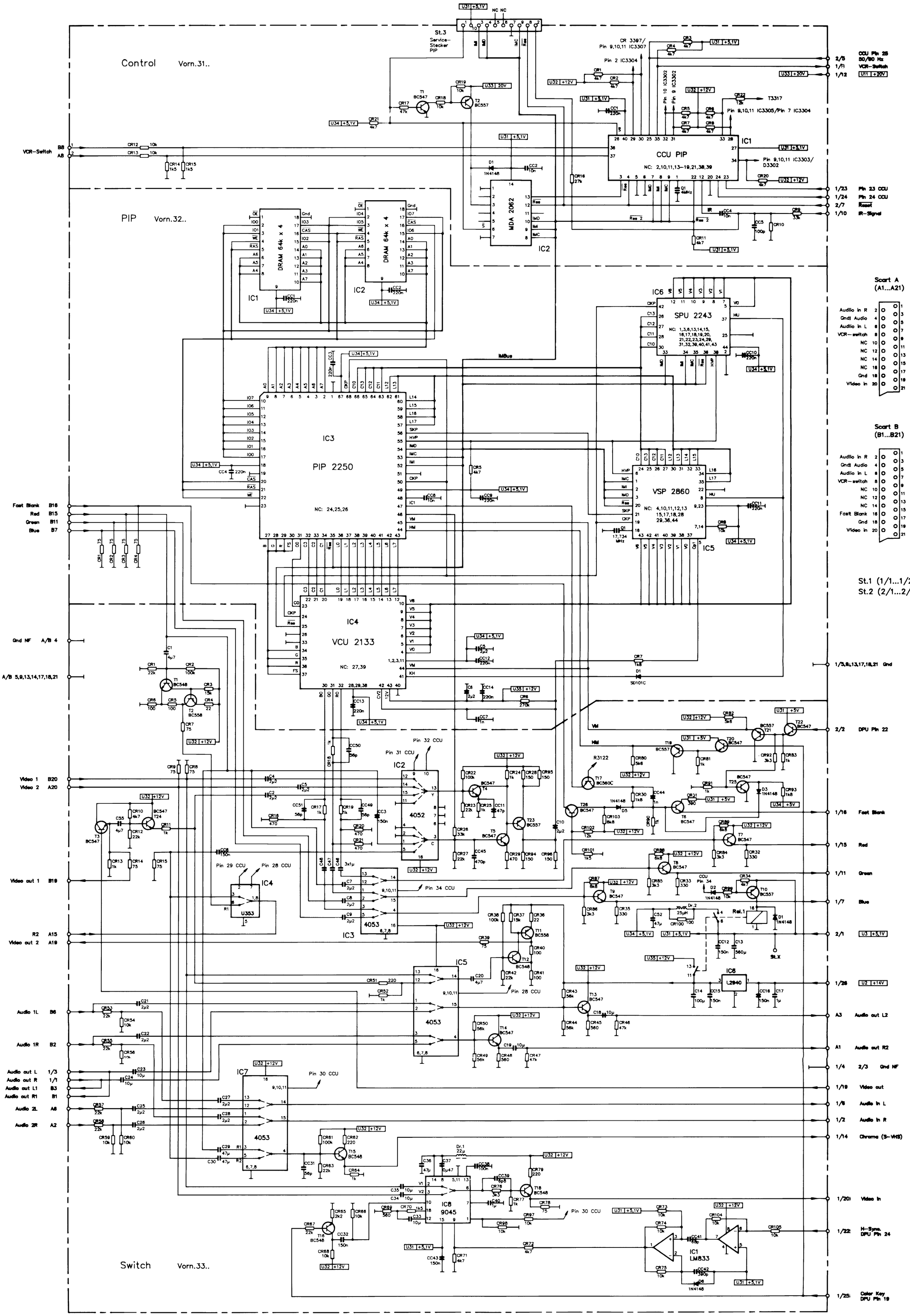
TIMEBASE 10 µsec/div
AMPL. 2 V/cm DC

Schaltbild DTV 2 PIP

Circuit diagram DTV 2 PIP

Die Positionsnummern auf der Leiterplatte und dem Schaltbild sind mit der entsprechenden Vornummer zu ergänzen.

The position numbers on the P.C.B. and on the circuit diagram have to be completed with the corresponding key numbers.



Schaltbild Signalteil DTV 2

Circuit diagram signal unit

Die Positionsnummern auf der Leiterplatte und dem Schaltbild sind mit der entsprechenden Vornummer zu ergänzen.

The position numbers on the P.C.B. and on the circuit diagram have to be completed with the corresponding key numbers.

Video
Vorn. 11..

Tuner + ZF
Vorn. 12..

Zentrale Steuereinheit
Vorn. 13..

Bedienteil
Vorn. 15..

Videotext
Vorn. 6..

Ablenkung
Vorn. 7..

Scart
Vorn. 8..

Audio Endstufe
Vorn. 9

Audio Digital
Vorn. 10..